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Research Article

Optimization of dual threshold MOSFET for 1-bit full adder cell

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Abstract

Power and delay is very important issue in low voltage and low-power application. In most of the digital circuit systems adder are in the critical path that affects the overall speed of the system. In this paper proposes a 10 transistor low power full adder cell with least NMOS and PMOS transistor count that helps to reduce the threshold loss problem. It increases the speed. By using Dual Threshold techniques to improve the threshold loss problem and reduces power consumption compare with other types of adders. Normally full adders need more area but the proposed circuits have negligible area. The threshold techniques are used for good voltage swing. BSIMv13.0 90 nm standard models are used for simulations on Tanner EDA tools.

Keywords: N-channel MOS; P-channel MOS; Gate diffusion input; Dual threshold; BSIM.

Introduction

The addition of numbers is performed using adders. ALU (Arithmetic and Logical Unit) is used in many computers and processors. A 1-bit numbers is add by using 1-bit full adder [1]. The critical path of full adders runs through both ex-or gates ends with carry bits C and sum bit S [2]. It takes 1 delays to complete while using ex-or gate , and then delay imposed by the critical path of a full adder is equal to $T_{FA}=2 * T_{XOR}=2D$.

The critical path of carry runs through one ex- or gate in adder and through 2-gates (AND and OR) in carry block and therefore, if AND or OR gates takes one delay to complete as a delay of $T_C= T_{EX-OR} + T_{AND} +T_{OR}=D+D+D=3D$. For reducing the transistor count Gate Diffusion Input (GDI) technique is used.

Proposed method

The present work is mainly focused to reduce the transistor count and threshold loss problem by using the GDI based Dual Threshold techniques. The Gate Diffused Input is used for reduces the P-channel MOS (PMOS) and N-channel MOS (NMOS) count.

GDI Technique

The drawback of CMOS and PTL (Power Transistor Logic) is eradicated by using GDI technique. This technique is mainly used for, while maintaining low complexity of logic design [3], power consumption, propagation delay and area of digital circuits. The transistor count also get reduces [4,5]. In low-power design technique under certain operating conditions in-cell swing restoration is the major advantage. By using GDI logic the XOR gate can design and implement in the 10 transistor logic. Normally GDI has three inputs G, P, N. G is Gate, P is PMOS and N is NMOS.

From the table 1 when A='0' and B='0' the transistor M1 and M3 will be ON and when A='1' and B='0' the transistor M1 and M4 will gets ON, but there is a threshold loss in the output. Dual threshold CMOS design is used for optimizing the switching speed and the power consumption is reduces. The different threshold voltage of switching is implemented for PMOS and NMOS MOSFETs.

GDI based dual threshold techniques

In GDI logic when input is given the performance of digital circuits is judged by its speed in producing output [5,6]. This technology is most common for designing digital circuit.

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The optimization is increased in the circuits in terms of speed when CMOS logic is developed [7]. Another techniques which reduces the number of transistor and increase the speed is Pass Transistor Logic (PTL). The parallel combination of NMOS and PMOS is done in Transmission Gate (TG) [8]. The Pass Transistor Logic (PTL) is replaced by GDI but slightly difference in CMOS design [9]. The advantages of PTL over CMOS is as follows.

Low power dissipation and lesser delay is by using less number of transistors.

Small area and less interconnection effect due to lesser number of transistors.

The two main problem in PTL is reduce circuit speed at low power operation and high static power dissipation. By using few transistor in low power circuits the GDI designed fast [10]. CMOS inverter structure similar to GDI cell. In CMOS inverter the PMOS source is connected to VDD and NMOS source is connected to GND. But in GDI cell this is not necessary, but it has some difference.

The following are three input in GDI namely; G : the gate f NMOS and CMOS is the common input, N : the source/drain of NMOS is given as input, and P : the source/drain of PMOS is given as input

To N and P the bulk of PMOS and NMOS are connected. The important difference between GDI and CMOS is that in GDI G, P and N terminals are given to the supply VDD or GND [10,11]. The supply and ground to PMOS and NMOS is not fixed in GDI. For normal full adder 26 transistor is needed, thereby it increase the power consumption, area and cost [6]. So GDI technique is used to reduce the number of transistors and power consumption, hence the delay has been decreased [11]. In GDI technique for full adder 11-transistors have been used.

In future technology, sub-threshold leakage current plays a major role in increasing the total power dissipation. So the dual threshold voltage is used for reducing power dissipation in combinational logic blocks of static and dynamic. The low threshold voltage is in evaluation mode and in high threshold voltage is in pre-charge mode. The different combinations of Threshold is tried in PMOS and NMOS to get better leakage power, average power and delay performance. Thereby for 11-transistor full adder the dual threshold is applied The fig. 1 shows the circuit diagram of 11-tansisitor full adder.

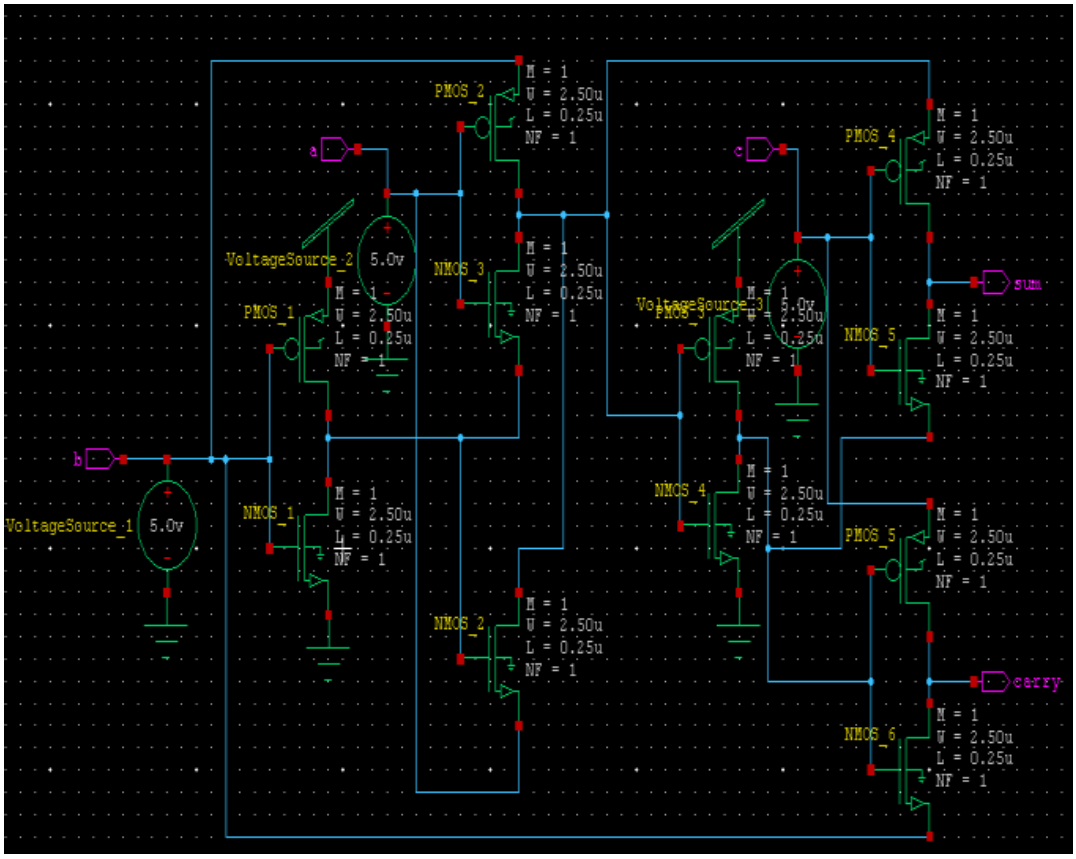

Fig. 1. 1-bit transistor full adder circuit

When low logic is in a and b signals, it turns on the added NMOS transistor where voltage is 0 when it discharges through F node. The proposed system reduces the low threshold loss, low power consumption, speedy, efficient noise immunity. The 11-transistor full adder design, the PDP is more efficient than conventional GDI full adder circuit. The cost is reduced and the power consumption is also decreased. to nullify the substrate bias effect the bulk terminals were connected to their respective source terminals. The dual threshold is applied in the voltage source 1, voltage source 2, voltage source 3 which is connected to the 3 inputs a, b and c of the full adder.

Results and discussion

In this section, the performance of the 11-transistor full adder is analyzed and the dual threshold is calculated using Tanner EDA tool on 90nm technology. The NETLIST shown below is the comment which is written to run the 11-transisitor full adder.

Netlist

```
.tran    5n
1
0
0
n        vs vdd GND 5
v1 a GND dc 5 BIT
({1010})
v2 b GND dc 5 BIT
({1010})
v3 c GND dc 5 BIT
({1010})
.print tran v(a) v(b) v(c) v(sum) v(carry)
.power vs 0n 100n
.end
```

In the line 2 vs is mentioned as voltage source name and vdd is mentioned as positive terminal and GND is as the negative terminal and 5 as the supply. The v1, v2 and v3 be the positive terminals. The input a,b and c have forced the 4-bit inputs as ({1010}) and the output which should be viewed is mentioned in the line

.print tran v(a) v(b) v(c) v(sum) v(carry)

which views the waves for the a, b, c, sum and carry.

Fig. 2 shows the simulation waveform of 11 transistor full adder circuit.

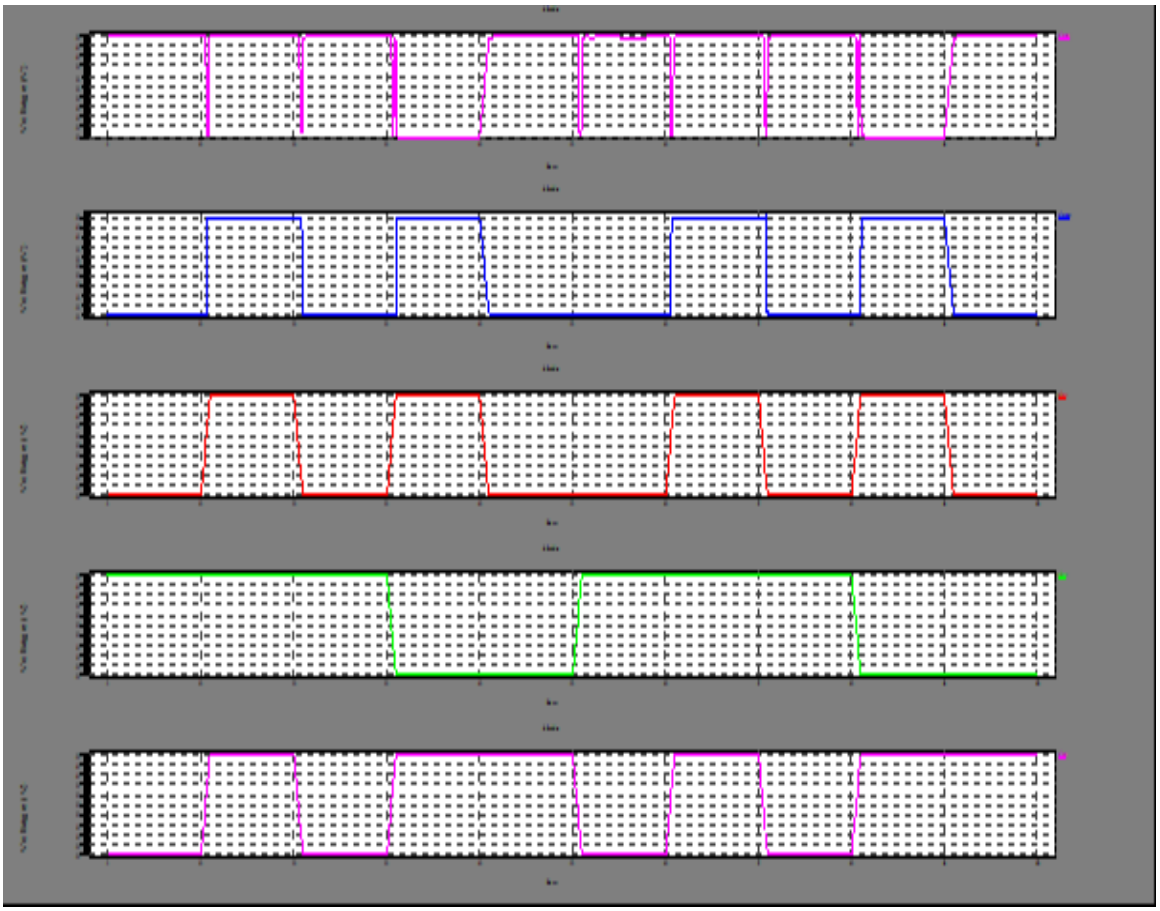

Fig. 2. Wave form of full adder

In this without using the voltage probe and the current probe, the waveform is got according to the NETLIST command.

Power results

vs from time 0 to 1e-007

Average power consumed -> 3.773193e- 005 watts Max power 1.367382e-003 at time 1.1e-008

Min power 1.438129e-009 at time 0

The fig. 3 represents the output waveform for the voltage source 1 by using current probe. The fig. 4 represents the output waveform for the voltage source 2 by using current probe. Fig. 5 represents the output waveform of voltage source 3 by using current probe. The fig. 6 represents the output waveform for the voltage source 1 by using voltage probe. The fig. 7 represents the output waveform for the voltage source 2 by using voltage probe. The fig. 8 represents the output waveform for the voltage source 3 by using voltage probe.

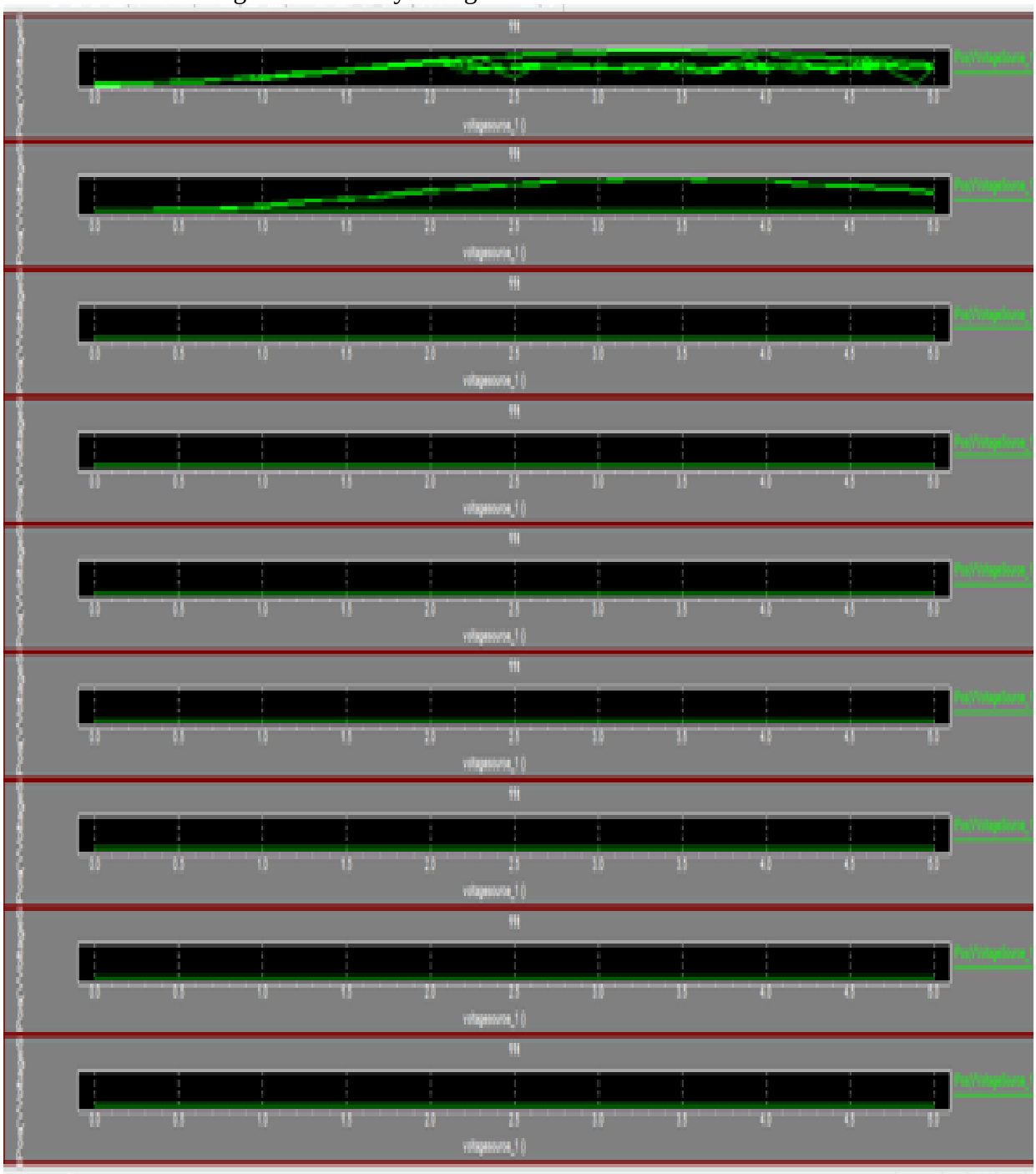

Fig. 3. Volatge source 1 by using current probe

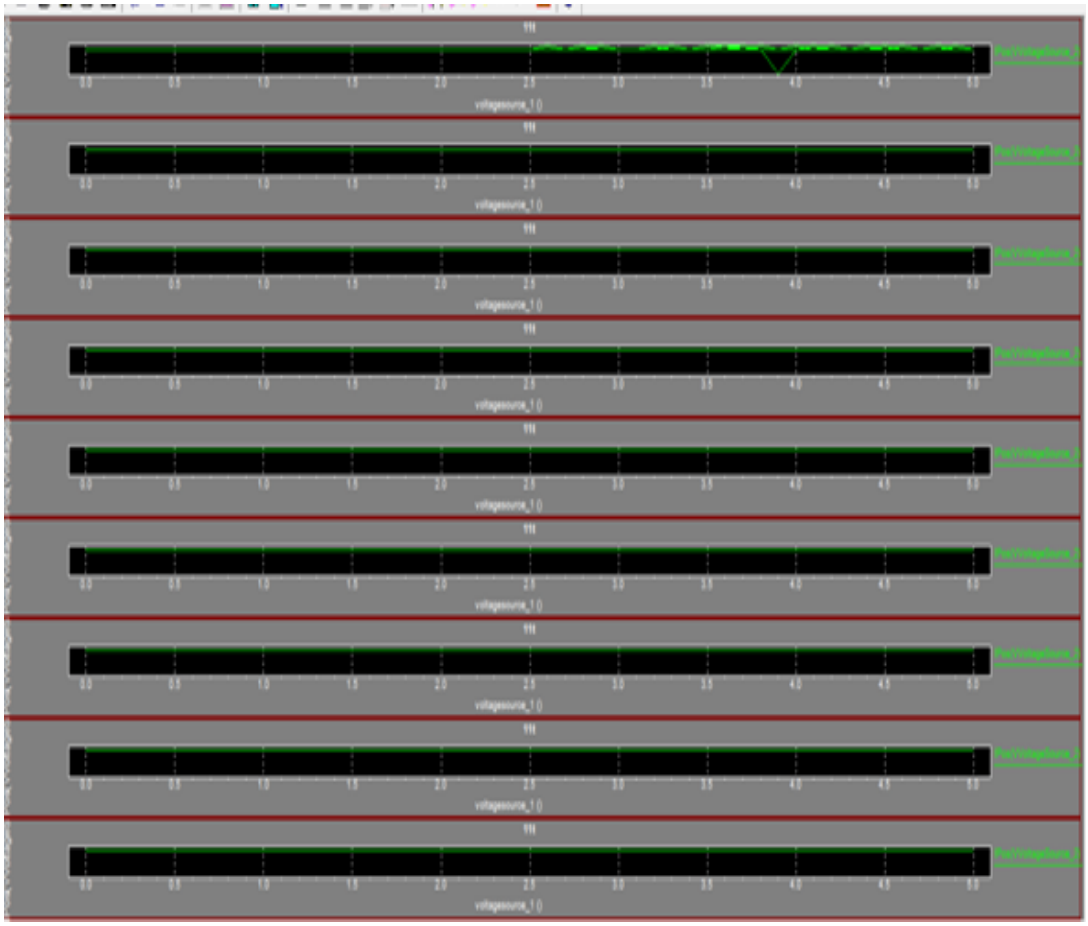

Fig. 4. Voltage source 2 by using current probe

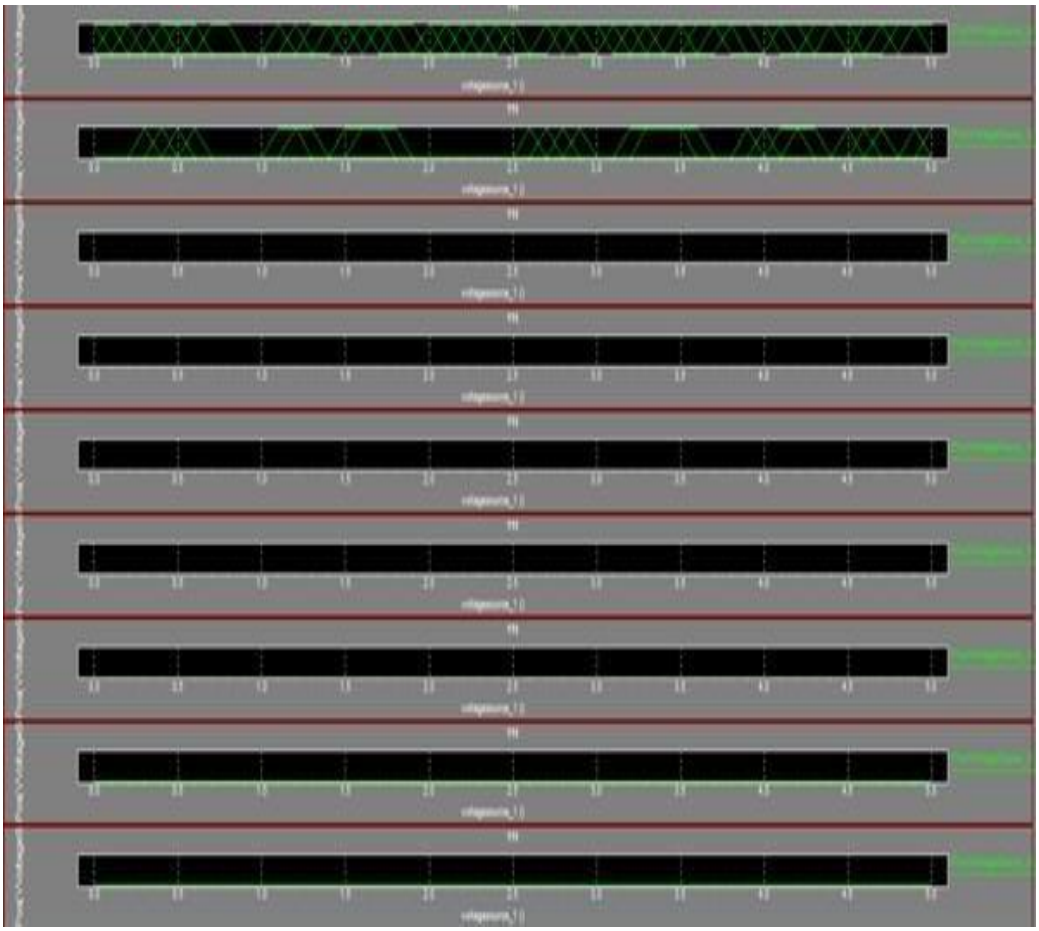

Fig. 5. Voltage source 3 using current probe

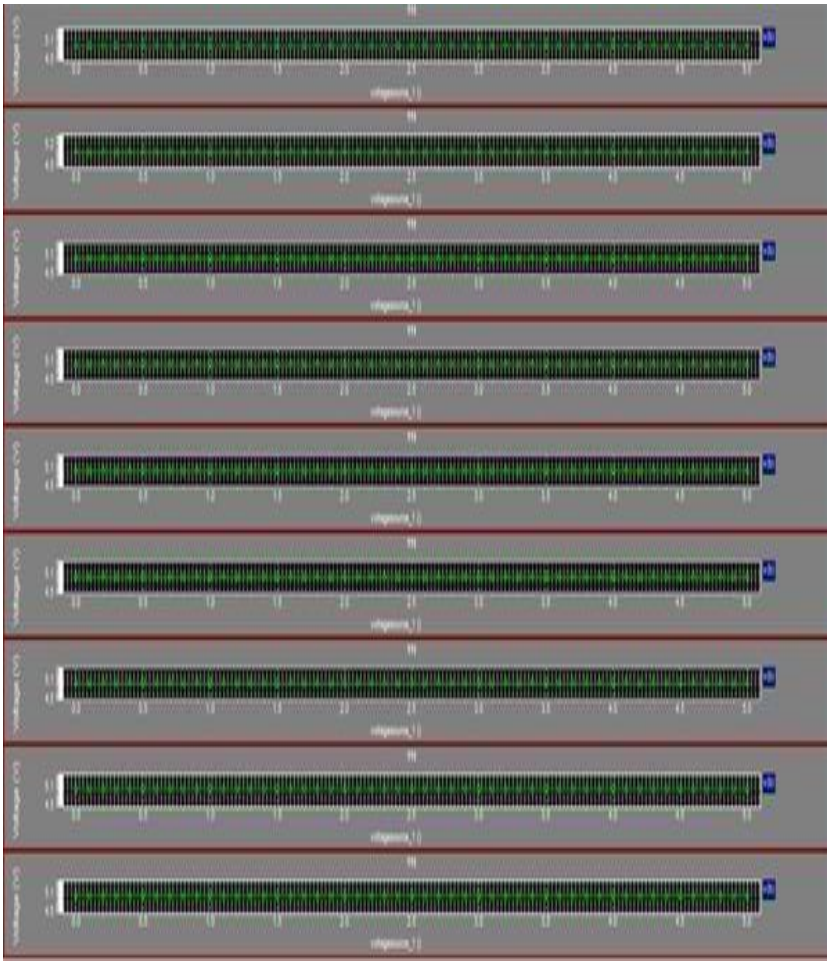

Fig. 6. Volatge source 1 by using voltage probe

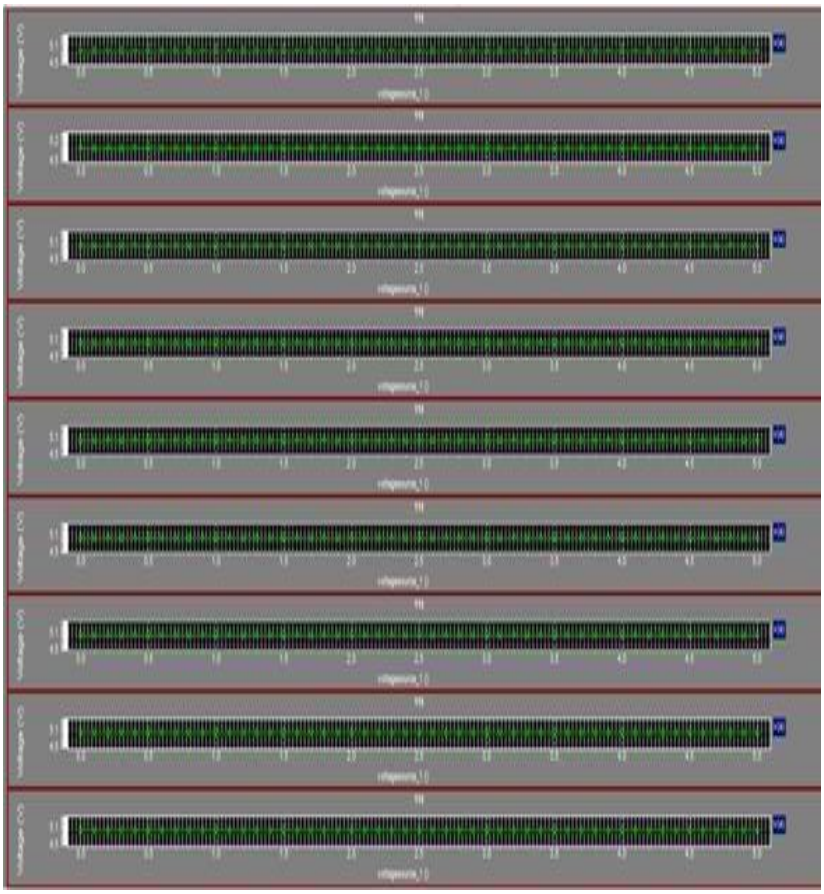

Fig. 7. voltage source 2 by using voltage probe

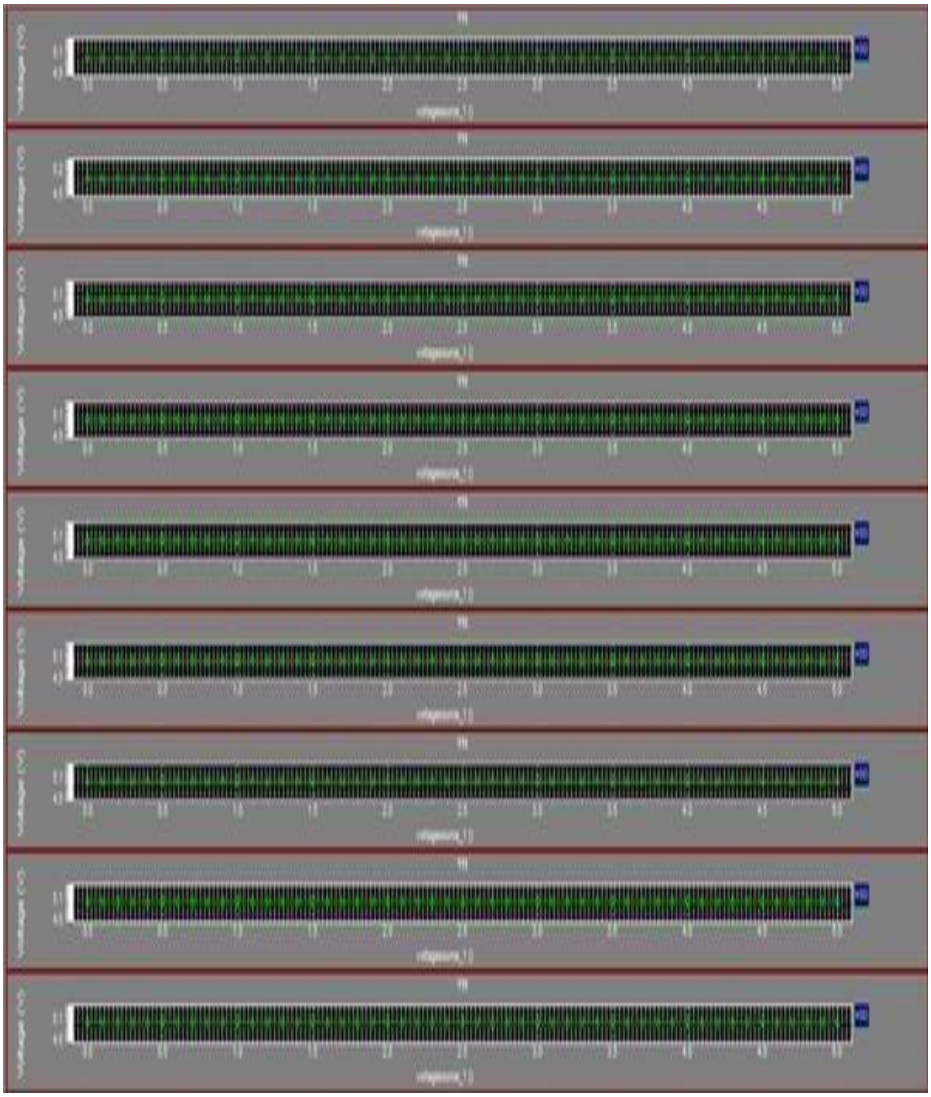

Fig. 8. voltage source 3 by using voltage probe

Conclusions

The performance of 11- transistor full adder circuit in GDI is more efficient than the normal CMOS full adder, which can operate at low voltage and good output swings. Power consumption of the 11- transistor full adder is decreased compared to CMOS full adder by verifying using power results. It was highest speed of operation that is with the low threshold MOSFET in PMOS and NMOS minimum delay is achieved by this circuit. To speed of operation is low that is with high threshold MOSFET in PMOS and NMOS maximum delay is achieved by the circuit .Here the power consumption is high and the leakage power is low. Thereby considering all the design constraints in the 11-transistor full adder circuit with low and high threshold MOSFET in PMOS and NMOS respectively.

Conflicts of interest

Authors declare no conflict of interest.

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