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Research Article

Design of ripple carry adder using pseudo-NMOS, dynamic circuits and pass transistor logic

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Abstract

The present work is mainly focused on area and power of ripple carry adder by using different types of circuit families like pseudo-NMOS logic, dynamic circuit logic and pass transistor logic are used. The main objective of this paper is to reduce the pull-up network or PMOS transistor counts. Because the flow of mobility of electron in PMOS is low so it takes more time. To reduce the PMOS counts, power consumption for RCA by using this logic. In pseudo-NMOS logic, instead of using every PMOS use only one PMOS that is connected to ground. In dynamic circuit logic, instead of connecting PMOS to ground to give clock signal to PMOS to reduce the static power dissipation. In pass transistor logic it uses only pull-down network that means NMOS logic so half of the transistor gets reduced. Based on these results we know that, which logic is efficient to construct the Ripple Carry Adder by using Tanner tool version 13.

Keywords: Dynamic circuits; Pass transistor; Pseudo NMOS; Ripple carry adder.

Introduction

In earlier method they did not considered the area. So area gets increased, the power dissipation is also increased [1]. In the work, authors we mainly focused on to reduce the area and power. We implement RCA by using three types of logics. Ripple carry adder is takes the carry-out from the full adder and give into succeeding adders. It is called a ripple carry adder because each carry bit gets rippled into the next stage. It uses a normal half adder and full adder circuits to implement RCA. We just construct normal half adder and then it converts into symbol [2,3].

By using half adder symbol and full adder symbol to implement the ripple carry adder. In this paper the ripple carry adder was designed by using pseudo-NMOS, dynamic circuits and pass transistor logic. In pseudo-NMOS logic there is only one pull up transistor is used instead of using several PMOS that means the area gets reduced and PMOS is connected to ground. In dynamic circuits here also only one PMOS transistor was used. Instead of connecting PMOS to ground the clock input voltage is given to input in PMOS to reduce the static power dissipation. In pass transistor logic only pull down transistors are used to implement the RCA [4,5]. Because the flow of mobility in NMOS is higher and also it reduce the transistor count.

Materials and methods

The present work is mainly focused on to reduce the PMOS transistor counts by using different circuit families [6]. The circuit families are pseudo NMOS logic, dynamic circuits and Pass transistor logic.

Pseudo NMOS

In pseudo-NMOS logic the inverter that uses a p-device pull-up or load that has its gate permanently ground [7]. An n-device pull- down or driver is driven with the input signal. In this logic static power dissipation will occurred when the output is low through the direct current path that exists between VDD and GND. Slow rising transition because pull-up network has low mobility compared to pull-down. Processing time is reduced so speed is high because we use only one pull- up network [8,9].

Dynamic circuits

Instead of using pseudo NMOS logic we go for dynamic circuits. In dynamic circuits the PMOS

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connected to the clock signal to reduce the power dissipation in CMOS circuits [10,11]. Here one more NMOS transistor is used to reduce the static Power dissipation which is called as footed type. The same pulse was given to footed type logic. In footed type logic the NMOS was connected to ground. The main drawback of this logic is it needs a clock for the correct working of the circuit and the output node of the circuit is VDD till the end of pre-charge [12]. In this logic static power dissipation will occurred when the output is low through the direct current path that exists between VDD and GND. Slow rising transition because pull-up network has low mobility compared to pull-down [13]. Processing time is reduced so speed is high because we use only one pull- up network.

Pass transistor logic

By using different logic gates, it reduces the transistors count by eliminating redundant transistors. Transistors are used as switches connected directly to supply voltages. This reduces the number of transistors, but it decrease the high and low logic levels based on the difference of voltage. NMOS devices are effective in to pass strong logic '0' but it is poor at pulling an input to VDD [14]. Hence when the pass transistor pulls a node to high logic the output only charges upto VDD-VTh. In this when B is '1', top the first transistor will turn on and pass the input A to output F. When B is low '0', second transistor will turns on and passes a '0'. It is used for designing regular arrays, such as ROMs, PLAs and multiplexers, and demultiplexers. It decreases the logic levels based on high and low voltages [15].

Simulation output

In Fig 1 shows the design of ripple carry adder using normal logic. a, b, c are the inputs to the full adder and s0, s1, s2 are the sum outputs and c0 is the carry output. In normal ripple carry adder it uses normal half adder and full adder. In half adder EX-OR gate and AND gate is required to generate sum and carry. In full adder OR gate and two half adder is required to generate sum and carry. The half adder circuit is converted into symbol and then the full adder was designed. There are 26 transistors are required to generate a half adder and full adder to implement in RCA.

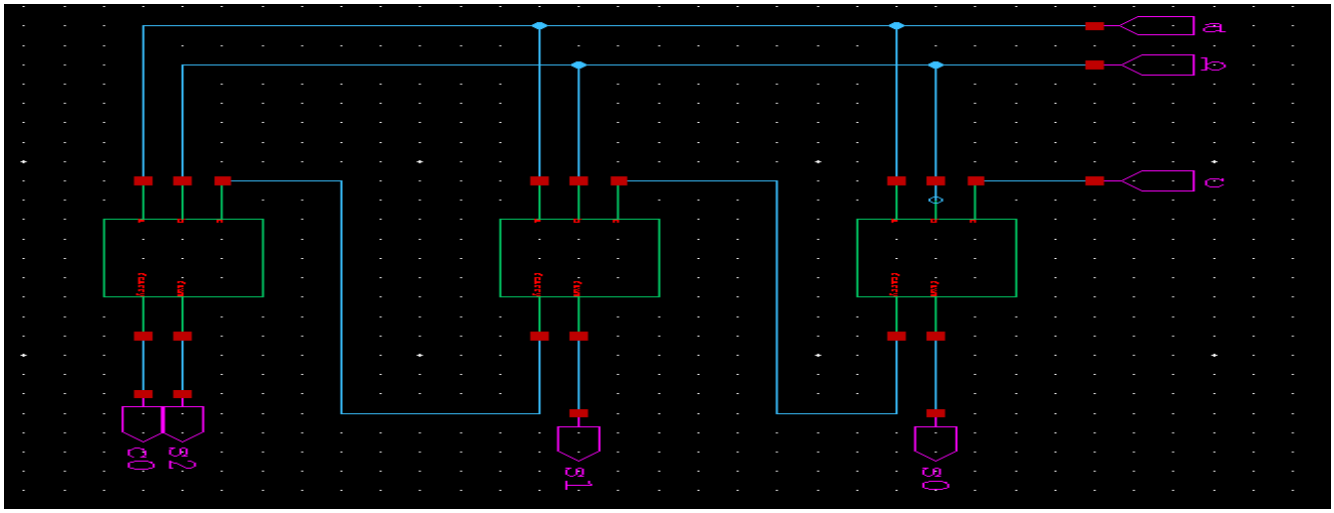

Fig. 1. Ripple carry adder design using normal logic

In Fig. 2 pseudo-NMOS logic the PMOS is connected to ground. Whenever the input gate input is '1' the PMOS will turned ON. So the Vout = VDD because PMOS is good for pass '1' logic and NMOS is good for pass '0' logic. There are 13 transistors are required for implement RCA by using pseudo-NMOS logic. In Fig. 3 additional input term PI was used for to give clock input signal to PMOS logic. There are two modes of operation occurred in dynamic circuits whereas pre-charge mode and evaluation mode. When the clock input (PI) is low '0' it works under pre- charge mode, and the clock input is high '1' it works under evaluation mode. There are 13 transistors are required for implement RCA by using dynamic circuit logic.

In Fig. 4 shows the pass transistor logic only NMOS or pull- down network was used. In pass transistor logic inputs are applied to source

and drain diffusion terminals. Here the width of the PMOS is taken equal to NMOS so that both transistors can pass the signal simultaneously in parallel. NMOS passes strong '0' weak '1'. They are not ratio devices, hence 5 minimum transistors can be used. They do not dissipate stand-by-power.

Table 1 shows the truth table for full adder. There are three inputs to the full adder A, B, Cin. SUM is the sum output and Cout is the carry output. Here Fig 5 shows the simulation output for RCA using normal logic. a, b, cin are the inputs to the full adder s0, s1, s2 are the sum output and cout is the carry output. There are 3 full adder are used to implement normal RCA based on the input values verify the simulation output by using table 1. Fig. 5, 6 and 7 shows the simulation output using pseudo-NMOS, dynamic circuits and pass transistor logic.

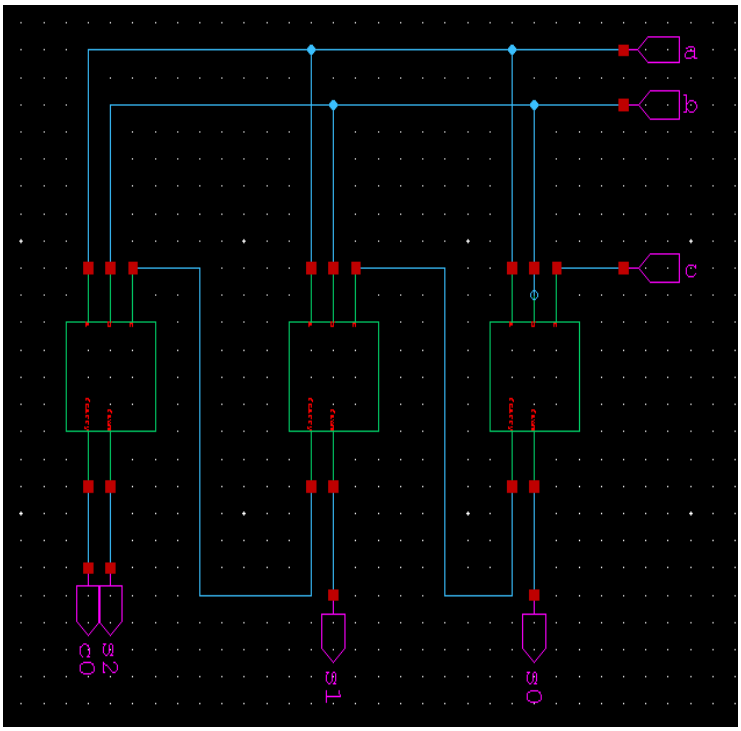

Fig. 2. Ripple carry adder design pseudo-NMOS Logic

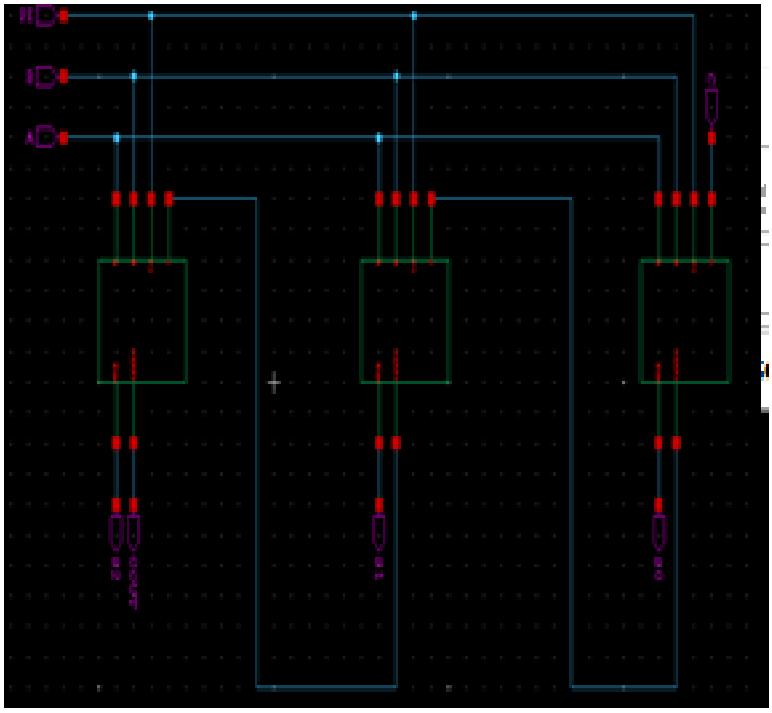

Fig. 3. Ripple carry adder design pseudo-NMOS Logic

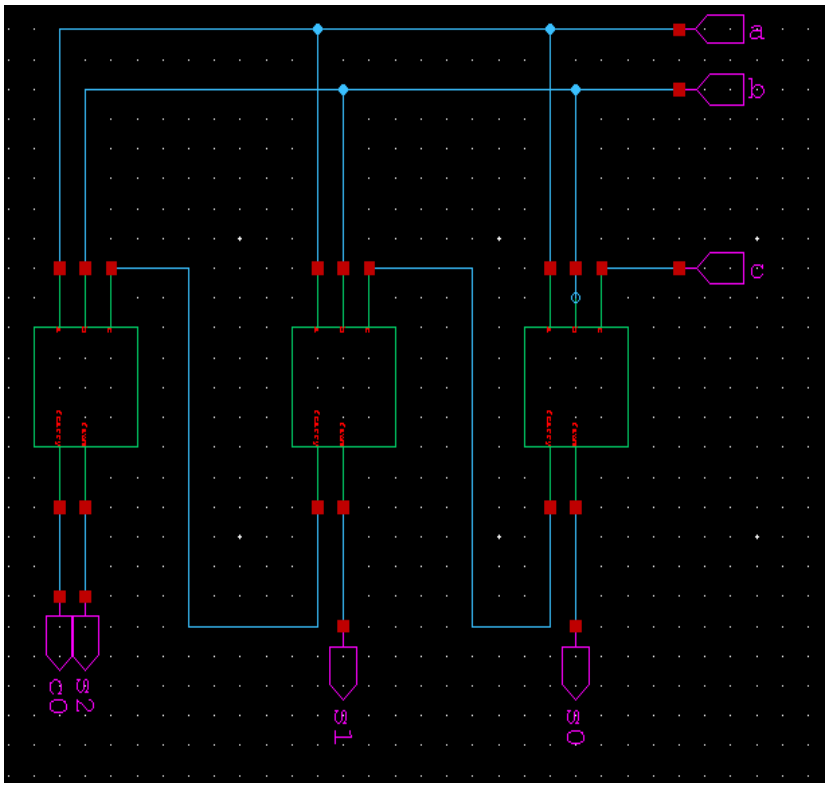

Fig. 4. Ripple carry adder design Pass transistor Logic

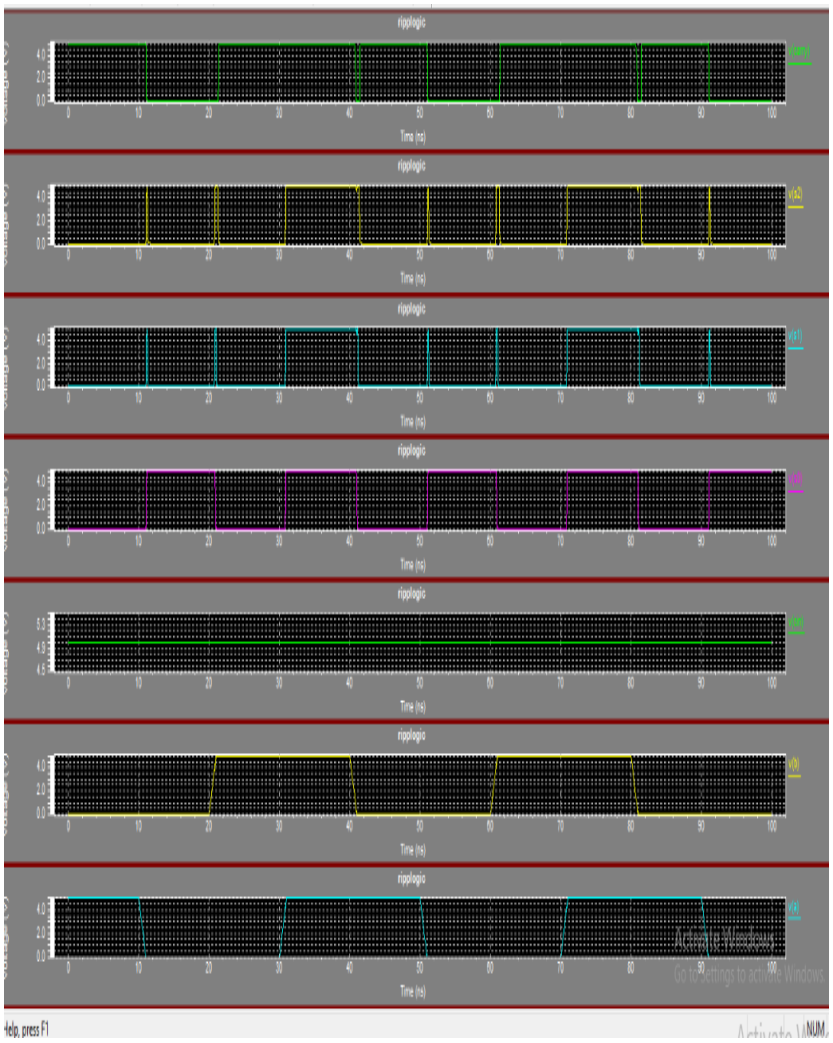

Fig. 5. Simulation output for normal logic

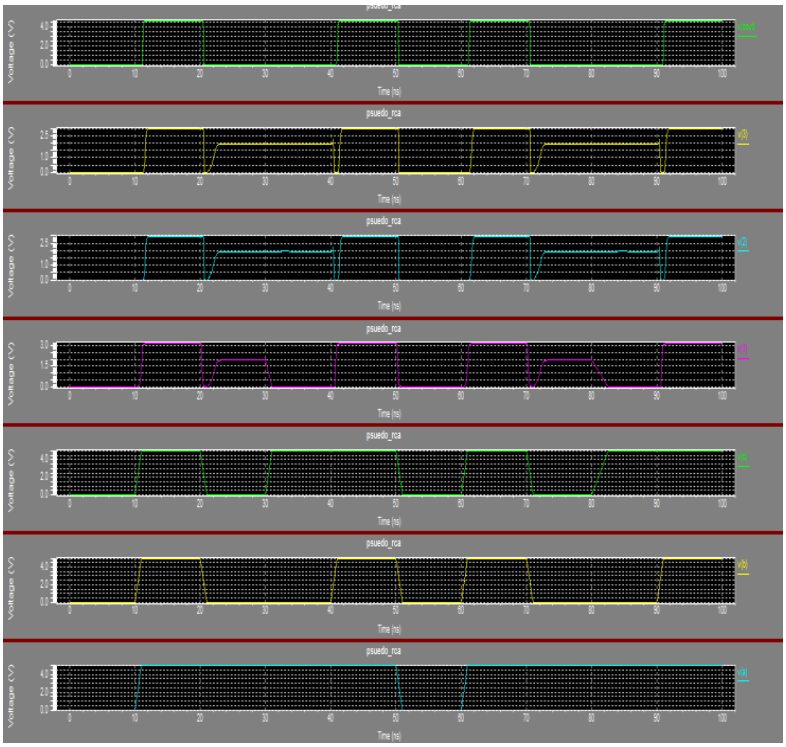

Fig. 6. Simulation output for pseudo-NMOS logic

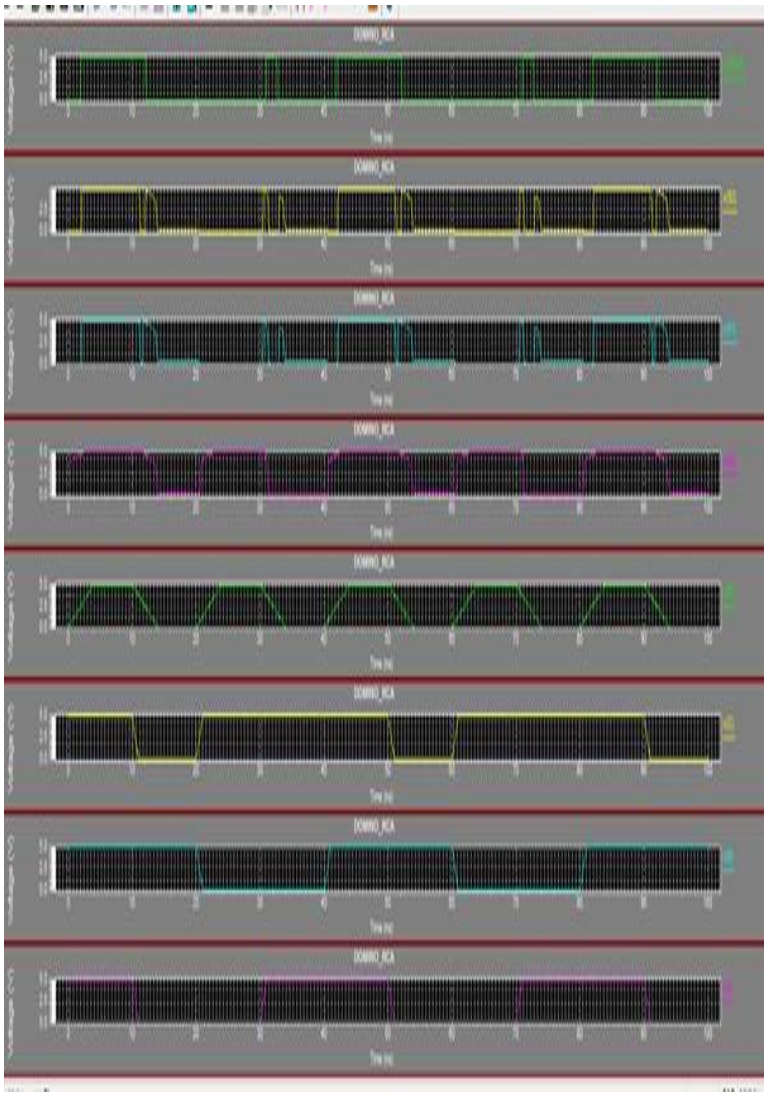

Fig. 7. Simulation output for dynamic circuits logic

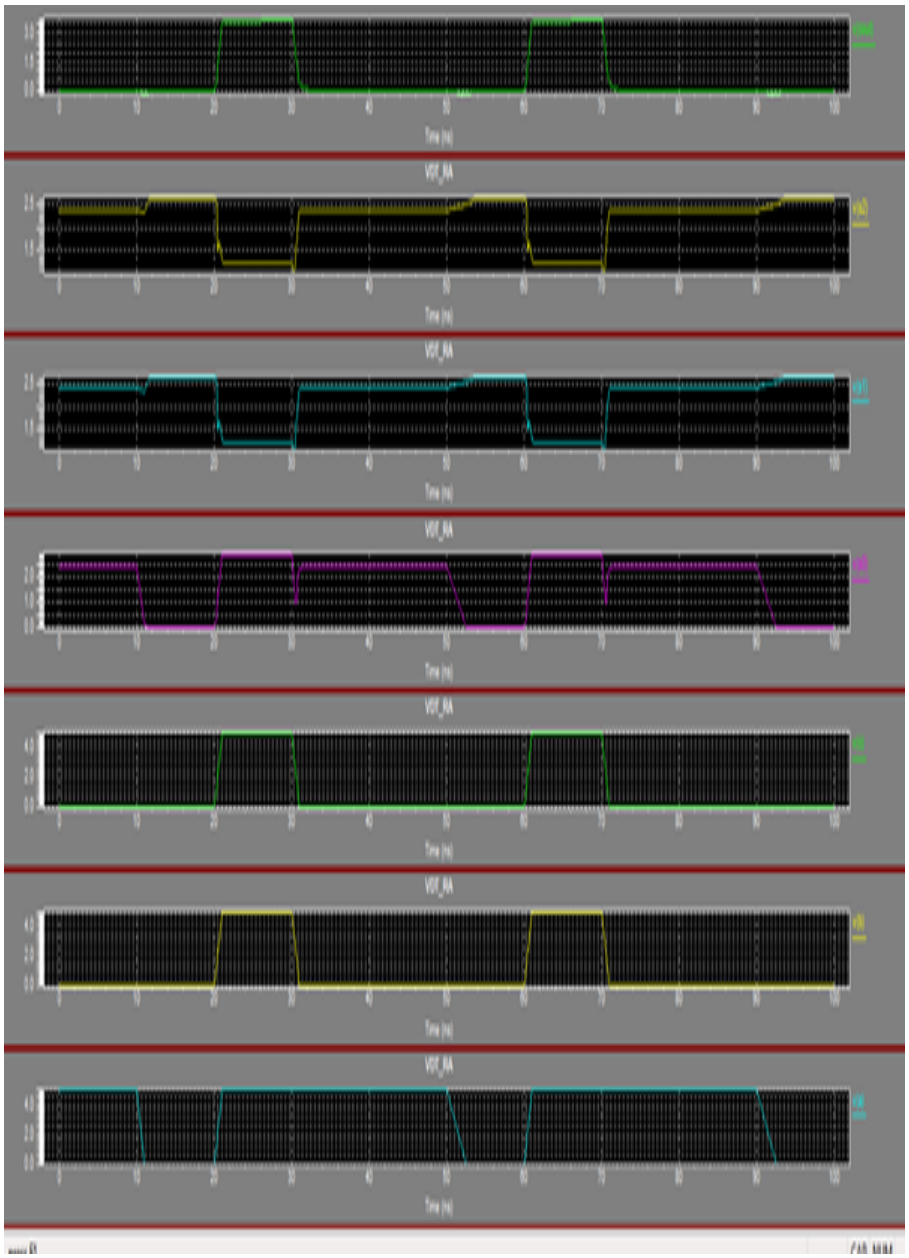

Fig. 8. Simulation output for pass transistor logic

Table 1. Full adder truth table

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Results and discussion

In the present work, authors compared the result and analysis which logic is very suited and efficient for to design a ripple carry adder by considering area, power and time (Table 2). By using normal full adder and half adder it requires 26 transistors and pseudo NMOS logic 13 transistors are required, dynamic circuits logic also it has 13 transistors. In pass transistor logic it has 5 transistors to implement RCA. In normal logic it takes 1.21 sec, 0.72 sec for pseudo NMOS logic, 2 sec for dynamic circuits and 1second for pass transistor logic. In terms of normal logic consumes 7.246 eW power, 4.080 eW power for pseudo NMOS logic, 4.97 eW power for dynamic circuits and 3.755 eW power for pass transistor logic. Based on the area, time taken and power the pass transistor logic is efficient compared with other circuit families. The area has been reduced by 84% and the power has been reduced by 48% when pass transistor logic is used to design RCA

Table 2. Comparison table of area, power and computation time

Circuit Families	Power (eW)	Area (No. of Transistor s)	Time (Sec)
Normal Logic	7.264	26	1.21
Pseudo NMOS	4.080	13	0.72
Dynamic Circuits	4.97	13	2
Pass Transistor	3.755	5	1

Conclusions

By comparing the area and power, the pass transistor logic is takes less area which means only five transistors are used to implement the ripple carry adder and power also gets reduced. In pseudo-NMOS and dynamic logic occupies more area and power compared to pass transistor logic. The area has been reduced by 84% and the power has been reduced by 48% when pass transistor logic is used to design RCA. Based on these parameters pass transistor logic is efficient to implement the ripple carry adder. In future we compute delay and reduced power Consumption for using different types of circuit families.

Conflicts of interest

Authors declare no conflict of interest.

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