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Research Article

Design of Low Power 180 nm Subthreshold 7T Non-Volatile SRAM

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Abstract

On-chip cache memories are present in every system on chip devices. These cache memories are made up of static random access memory (SRAM). Low power and High speed are the constraints placed on the SRAM cell design. The increased importance of lowering power in memory design has produced a trend for operating memories at lower supply voltages. The implementation of conventional 6T SRAM memory is scaling to newer technology as it operated in the deep submicrometer region has become difficult due to the compromise between area, power, and performance. To overcome the read-write conflicts 7T cell is proposed. The 7T cell is operated at the 0.4v and can also achieve the low area per bit cell by using 0.18µm Technology. The 7T static random access memory has improved read and write stability and noise margin free read operation also in the sub-threshold region.

Keywords: Cache memory; Low power; Seventransistor (7T); SRAM; Subthreshold; Noise margin.

Introduction

Semiconductor Electronics has significantly dominated the Industry as well as the domestic side. Along with the advancements in microelectronic technology, revolutionary changes have taken place in a short span of time. On recent deep sub-micrometer technology nodes, the scaling of transistors in digital design to decrease power and improve performance has become a significant challenge. With the decrease in technology node, the circuits become more vulnerable to variability and noise. A 7T SRAM operated in sub-threshold area with improved read and write margin. The accomplishment of 6T SRAM in deep sub-micrometer region lags in terms of read and writes stability. The correlations between the dynamic stability and static margins were observed greatly and the extra PMOS drain fighting [1,2]. This can be achieved by using the two boosting capacitors connected to BL and BLB [3].

It gives improved read margin and superior access device strength. A 5T bit cell that uses asymmetric sizing to get better the read stability and to give the trade off for other metrics such as area, write noise margin, read current and also the leakage current.[5,6 **]** The vacillation in the electrical characteristics of small geometry SRAM cell transistors are established to limit the yields and least amount operating voltage of conventional CMOS SRAM arrays [4]**.**

The new 7T dual-VT static random access memory is implemented which concurrently reduces the active and standby made power consumption while enhancing the data stability and the read speed. A new average 7TIR nonvolatile SRAM for low power application which improves the read and write margin as well as the restore energy by using the source switch transistor the energy minimization for circuits which are operating in the sub threshold region were superintendent **[7**,8]. Static Noise Margin variations are observed [9,10]. The SNM is the maximum amount of voltage noise that can be introduced at the outputs of the two inverters such that the cell retains its data they presented the data retention voltage estimation. One of the best ways for leakage power reduction is to reduce the stand by supply voltage to a minimum level by the DRV[11].

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Subthreshold operation

The digital circuit design operated in the subthreshold region has emerged as a low energy solution for applications with strict energy constraints. Analysis of sub-threshold designs has focused on logic circuits for example, SRAMs comprise a significant percentage of the total area for many digital chips as well as the total power. For this reason, SRAM leakage can dominate the overall leakage of the chip, and largely switched capacitances in the bit lines and word lines make SRAM accesses costly in terms of energy.

The performance of SRAM operation into the sub-threshold region reduces both leakage power and access energy. It is also used for system integration; SRAM must become capable of operating at sub threshold voltages that are compatible with sub-threshold combinational logic.

Existing system

The architecture of the proposed asymmetric 7T cell is shown in figure 1. It comprises of an inverter-(PUR-PDR) and a pull-up pMOS (PUL), which are coupled together to store one-bit information An access transistor (ACL) is used for a single- ended write operation and two nMOS (R1, R2) to perform a single-ended read operation.

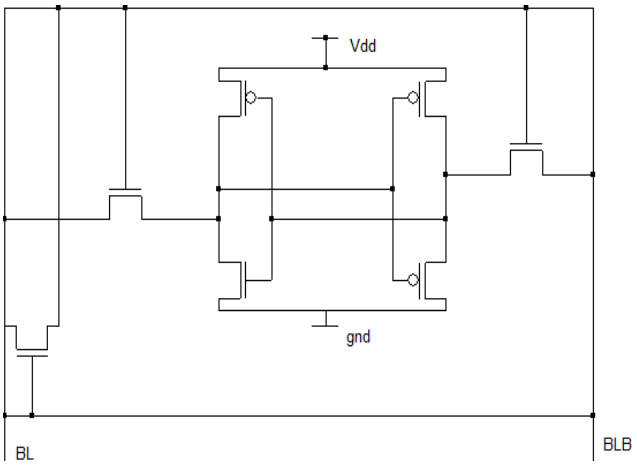

Figure 1. Proposed 7T SRAM cell

The write bit line (WBL) and write word line (WWL) are used for performing write operations, and the read bit line (RBL) and read word line (RWL) is used for performing a read operation. A nMOS (DL) with its gate terminal connected to ground potential is implemented to provide stability through leakage currents. Memory arrays are an important source of leakage since the majority of transistors are utilized for on-chip caches in today's high-performance microprocessors. The design of a low leakage SRAM cell with enhanced data stability is, therefore, highly desirable.

The SRAM array has been the industry standard due to its fast differential sensing and very low area. However, the extensive scaling of supply voltage has affected the performance of the read and writes operations in SRAMs, thereby making it difficult to implement the conventional 6T cell.

Write Ability

A single-ended write operation is more difficult to perform than the double-ended one in the conventional 6T cell. This is because a conventional 6T cell uses complementary bit lines to perform a write operation and either of the nodes (X or XB) in the cell is discharged quickly through its corresponding bit line. The 7T-C cell accomplishes a write operation through its single bit line, by relying entirely on the mutual effect of inverters to flip the values. Thus, writing ability in the 7T-C cell is achieved by modifying the voltage transfer characteristics (VTC) of each inverter. The trip point of one inverter is increased while the trip point of the other is decreased. The conventional 6T SRAM cell is able to maintain write ability down till only 800 mV, while the proposed cell maintains the write margin even at 400 mV. Also, the method of improving write margins for the 7T-C cell by resizing the transistors increases area.

Hold state

In the existing cell, as the DL transistor remains in cut off, the X node rises by a small voltage. during hold "zero" state, reducing the hold noise margin and making the hold "zero" state more vulnerable. If the X node voltage was to rise beyond the trip point of the PUR-PDR inverter, the cell data would be destroyed. In order to achieve the lowest X node voltage during hold "zero" state, the effective OFF-state resistance from X node to GND must be minimal in comparison to the OFF-state resistance of PUL. This can be achieved by implementing a combination of a wider access transistor (ACL), a longer pull-up transistor (PUL) and an LVT DL.

Proposed 7T SRAM cell

The schemes of the proposed 7T SRAM and the structure of NVSRAM with column-shared technology are shown in figure 2. The proposed AVE-7T1R also utilizes an RRAM with a switch transistor RSWL and two differential power rails. The salient feature of the proposed structure is the additional column-shared virtual switch transistor (SN) connected to the source of the driver transistors (DL and DR), which is area-efficient and in favor of writeability. During the SRAM mode operation, the control signal CTRL of SN is low- and high-voltage level of write and read operations, respectively. As a result, for a write operation, the write ability is significantly improved due to the isolation between the cell core and VSS source.

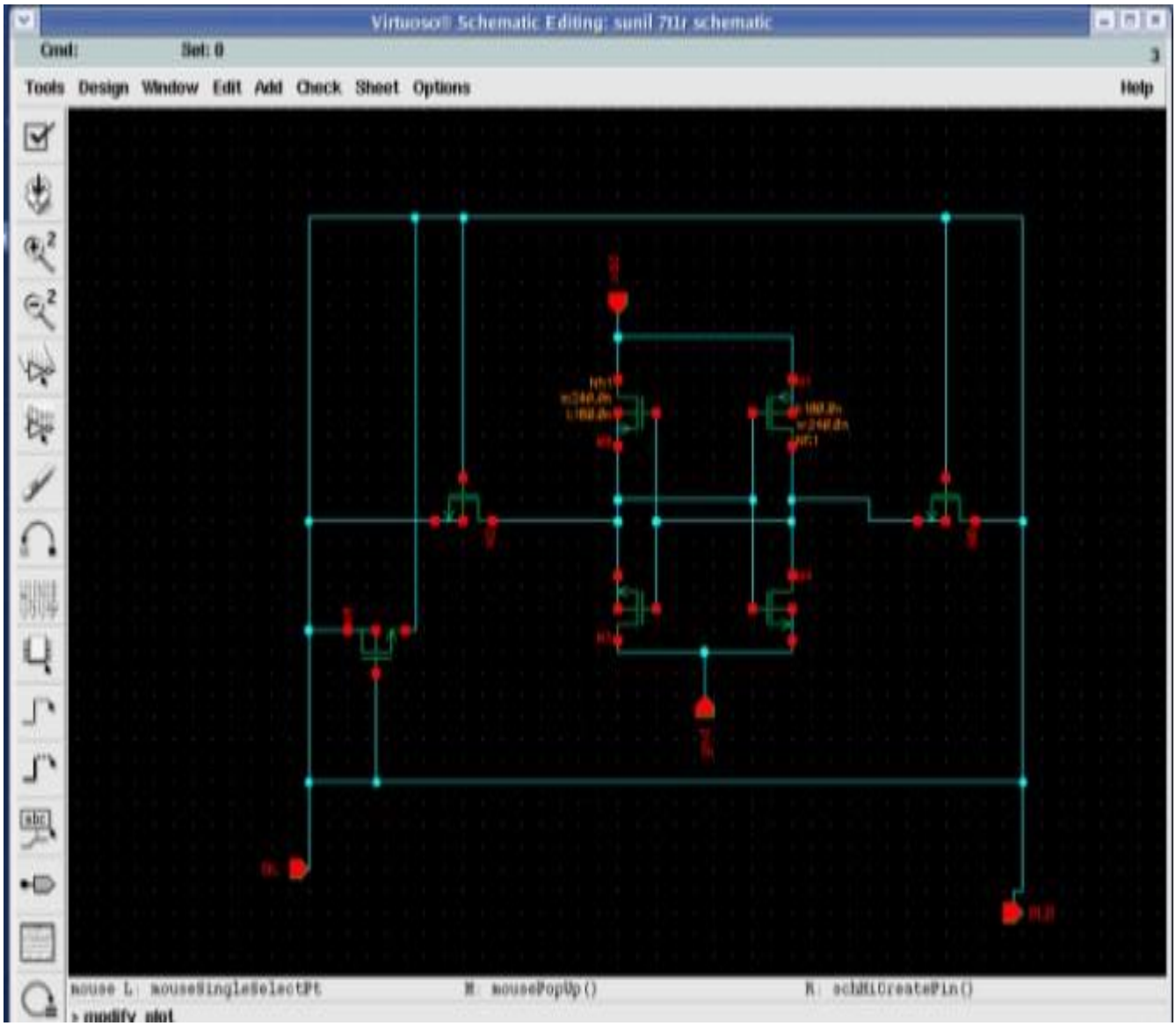

Figure 2. Scheme of the pproposed 7T SRAM cell design

Simulation results of the proposed 7T SRAM cell are shown in figure 3. Thus, the stability of R/W will be simultaneously enhanced by using the proposed structure. However, during the write operation, the hold static noise margin (SNM) of the column half-selected cells will be reduced, because they are temporarily isolated with the VSS caused by the low CTRL. Actually, the node VS will be rapidly recovered low state by the selected cell during the write operation, which should be beneficial for the trade off design.

Conclusions

In the present work, we proposed a new 7T non-volatile SRAM cell and it provides the area efficient memory which is used for low power application. It is shown that the proposed circuit

shows better read margin (RM) and write margin (WM). The proposed 7T SRAM cell operates in the ST region down to 0.34V. It decreases the area and thereby increasing the performance, the effectiveness of the 7T SRAM cell gives the significant data stability enhancement and leakage power reduction.

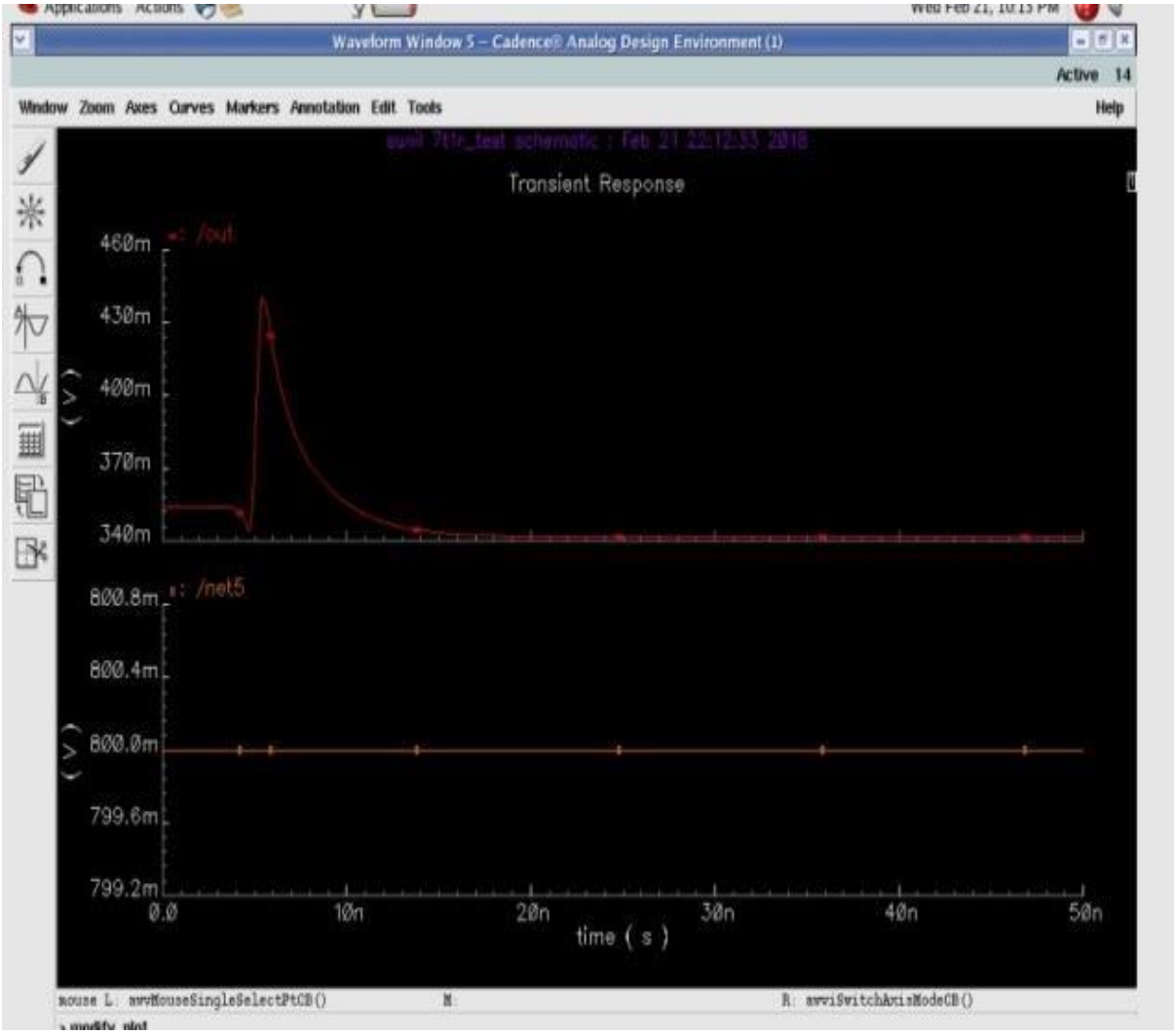

Figure 3. Simulation results of the proposed 7T SRAM cell

Conflicts of interest

Authors declare no conflict of interest.

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