



Research Article

Design of Power-Efficient and Wide-Range Voltage Level Shifter

S. Ramya*, R. Vishnu Priya

Department of Electronics and Communication Engineering, Arasu Engineering College,
Kumbakonam – 612501. Tamilnadu. India

*Corresponding author's e-mail: vimalandr@gmail.com

Abstract

The present work presents a wide-range and low-power voltage level shifter for efficient performance in dual-supply applications. The proposed circuit is made efficient by varying the strength of pull-down and pull-up transistors. The width/length ratio is varied, i.e., width/length (strength) is increased for pull-down transistors and decreased for pull-up transistors. This approach is based on the fact that the strength of the pull-up device is lowered while the pull-down device pulls the output down. At the same time, the pull-down device's strength is increased by an auxiliary circuit that consumes low power. The proposed circuit is simulated in 0.18 μ m technology Cadence Virtuoso software. The simulation results show that the proposed circuit can convert extremely low level of input voltage into high output voltage level. That is, it can convert low input voltage $V_{DDL}=0.7V$ to high output voltage $V_{DDH}=3V$ with power dissipation of 1.9314 μW .

Keywords: Voltage Level shifter; Low power; Efficiency; Power dissipation; Voltage range.

Introduction

Static power dissipation and dynamic power dissipation are some sources of power consumption. In digital circuits, we can reduce this static power and dynamic power dissipation by reducing the power supply voltage [1-3]. But the propagation delay of circuits increases while lowering the power supply voltage. In moderate-speed digital circuits or mixed-signal circuits, some parts operate at high speed; while some parts operate at low speed. In such circuits, instead of reducing the power supply voltage, we can use dual-supply architectures in which two supply voltages are used: low supply voltage (V_{DDL}) and high supply voltage (V_{DDH}). V_{DDL} is supplied for blocks that operate at low speed, i.e., that are in non-critical paths and (V_{DDH}) is applied for those digital blocks that operate at high speed, i.e., in critical paths [2,3]. In such a digital system with dual-supply architectures, voltage level shifter circuits are necessary so that they can convert the lower voltage levels into higher voltage levels to provide the needed voltage levels for the next blocks. To enhance the performance of the dual-supply systems, and

to avoid the degradation of their performance, the voltage level shifters used should be designed with reduced propagation delay, low power consumption and reduced silicon area. And also to save more power, the voltage level shifters should be capable of converting very low V_{DDL} values to values below the input transistors' threshold voltage. Therefore, in this paper, an efficient and low power voltage level shifter is proposed. This proposed shifter can convert even very low input voltages into high voltages at the output.

Existing system

Some of the conventional voltage level shifters are shown in Fig. 1. Fig. 1a shows a conventional voltage shifter. Its operation is given below. When the input IN is high, i.e., $IN=V_{DDL}$, the transistor MN1 is ON and pulls down the node Q1; MN2 is OFF. Next, MP2 is slowly turned ON and pulls up the node Q2 to V_{DDH} and then turns OFF MP1. Similarly, When the input IN is low, i.e., $IN=V_{SS}$, the operation is reversed. It is observed that in this circuit, contention is present at the nodes Q1 and Q2 between the PMOS devices (MP1 and MP2)

which are supplied by V_{DDH} and the NMOS devices (MN1 and MN2) supplied by V_{DDL} . So, when the difference between V_{DDL} and V_{DDH} is high, and when the input voltage is below the threshold range, this conventional circuit cannot convert the input voltage levels. Because the currents of the NMOS transistors are smaller than the currents of the PMOS transistors. To overcome this drawback, many attempts have been made. One such approach is to make use of strong PMOS devices by using low threshold transistors and weak NMOS devices by using high threshold transistors [4]. Another attempt is to employ strong NMOS devices by increasing the width of them. This will increase power consumption and also delay [5-9].

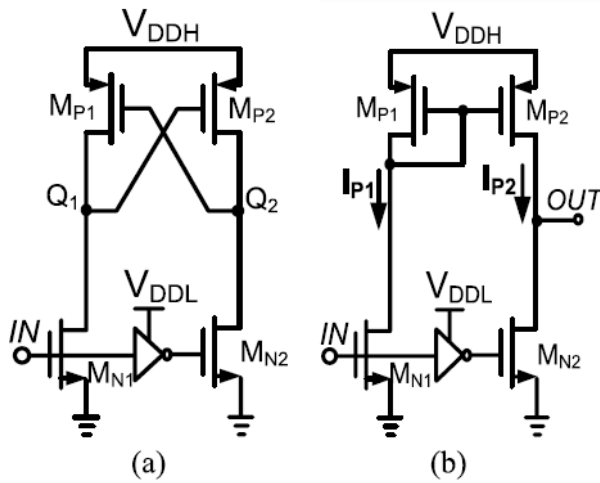


Fig. 1. (a) Conventional voltage level shifter and (b) voltage level shifter with a semi-static current mirror

The final approach is to lower the strength of pull-up transistors while the pull-down transistors are pulling the output down. The circuit shown in Fig. 1(b) employs a semi-static current mirror. It limits the current and this reduces the strength of PMOS transistor (MP2) while the NMOS transistor is pulling down the output. But this circuit has the drawback of static current which flows through MN1 and MP1 when the input signal is high. To reduce this static power consumption, a dynamic current generator may be used. This generator will turn ON at the transition times only [10-14].

Proposed system

To overcome the drawback of contention in the existing system, the transition current (I_{P1} and I_{P2}) should be avoided when the transistor MN2 pulls the output down. This is achieved by the proposed circuit given in Fig. 2. Its operation

is as follows. When the input goes to HIGH, MN1 turns ON and MN4 turns OFF. MN4 turns ON when OUT does not correspond to input because the overdrive voltage of MP3 is driven by a voltage (i.e., V_{DDH}) larger than that of MN3 (i.e., V_{DDL}). Thus, a transition current flows through MP1, MN1 and MN4. This current is mirrored into MP2 and pulls the output node up and MP3 turns OFF. Also, MN4 gate is pulled down which means that there is no static current through MP1, MN1 and MN4. If the aspect ratio of MP1 is chosen smaller than the aspect ratio of MP2, the power consumption can be reduced [15]. During the transition of input signal from high to low, MN2 turns ON and MN1 turns OFF at the same time. Hence, there is no transition current through MP1. Thus, the strength of pull-up device MP2 when the pull-down device pulls the output down. Therefore, the delay, contention and power consumption are reduced. Also, the shifter can correctly work for input voltages in the sub-threshold range. This principle is made possible using an auxiliary circuit in the proposed circuit. The auxiliary circuit consists of six transistors MN5, MN6, MN7 and it turn ON only when the input signal changes from high level to low level.

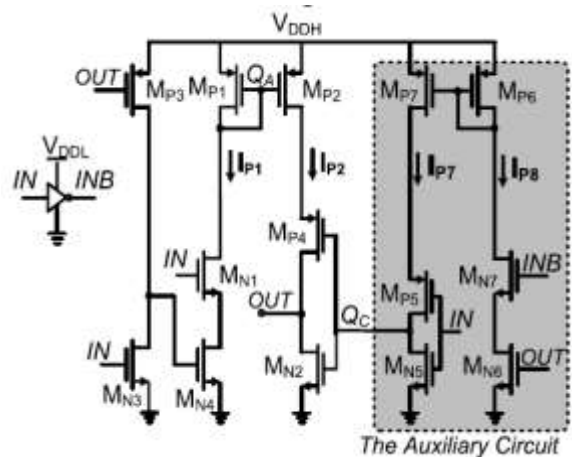


Fig. 2. Proposed voltage level shifter

The auxiliary circuit's operation is as follows. When the input goes low, and when the output does not correspond to input, MN5 turns OFF and MP6, MN6, MN7 are ON. Thus, a transition current will flow through MP6, MN6 and MN7. This current is mirrored into MP7 which pulls the node QC. That is MN2 turns ON and MP4 turns OFF and the contention is reduced significantly. When the output is pulled down to ground, MN6 turns OFF and no current is flowing through MP6, MN6 and MN7 which

means that the auxiliary circuit is ON only for the transition of the input from high level to low level. Thus the contention is negligible and the propagation delay and power consumption are reduced significantly. The proposed level shifter can be modified by increasing the strength of pull-down devices. The pull-down devices' strength can be increased by increasing their width.

Results and Discussion

The proposed level shifter (Fig. 2) and conventional level shifters (Fig. 1(a) and (b)) have been simulated in Cadence Virtuoso platform in 0.18 μm CMOS technology. The implementation of schematic of conventional level shifter (Fig. 3), simulation and experimental results are discussed. In the level shifter in Fig. 3, V_{DDL} of 1.5V and V_{DDH} of 3V are applied and the circuit is simulated in Cadence tool. The simulation result is shown below in Fig. 4.

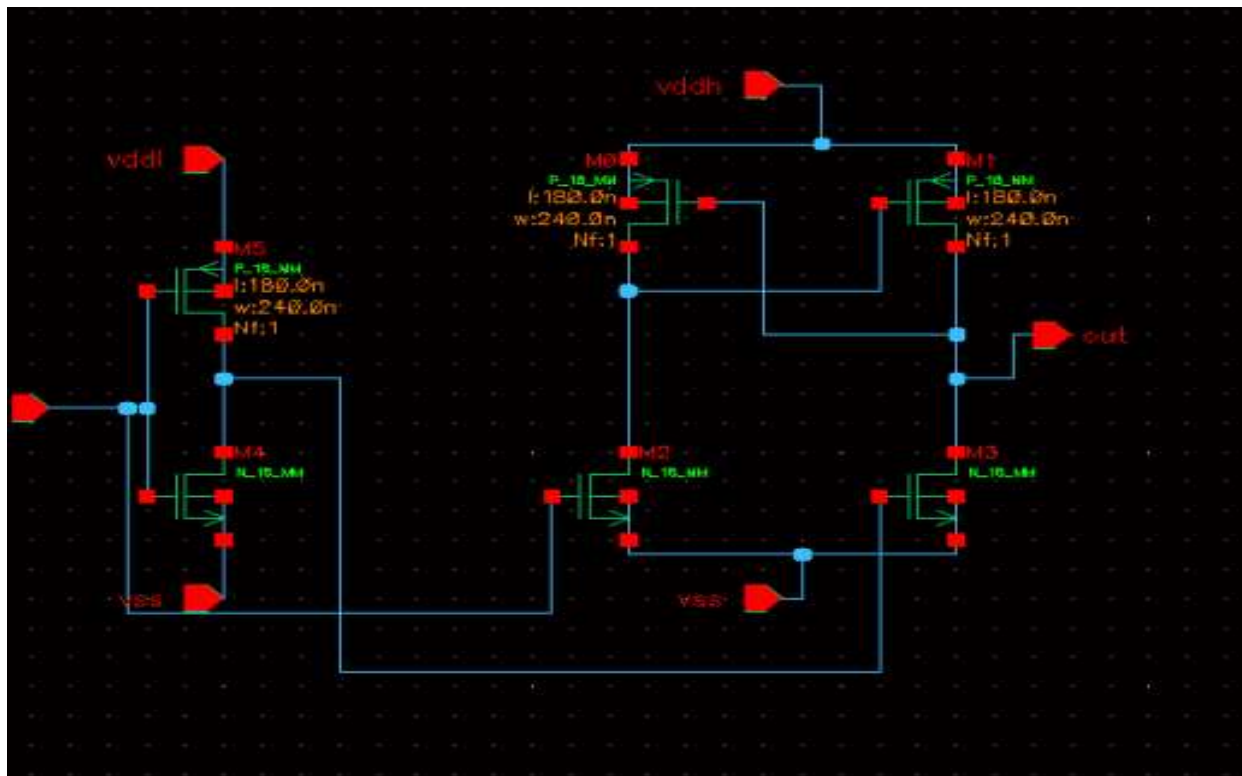


Fig. 3. Implementation of schematic of conventional level shifter

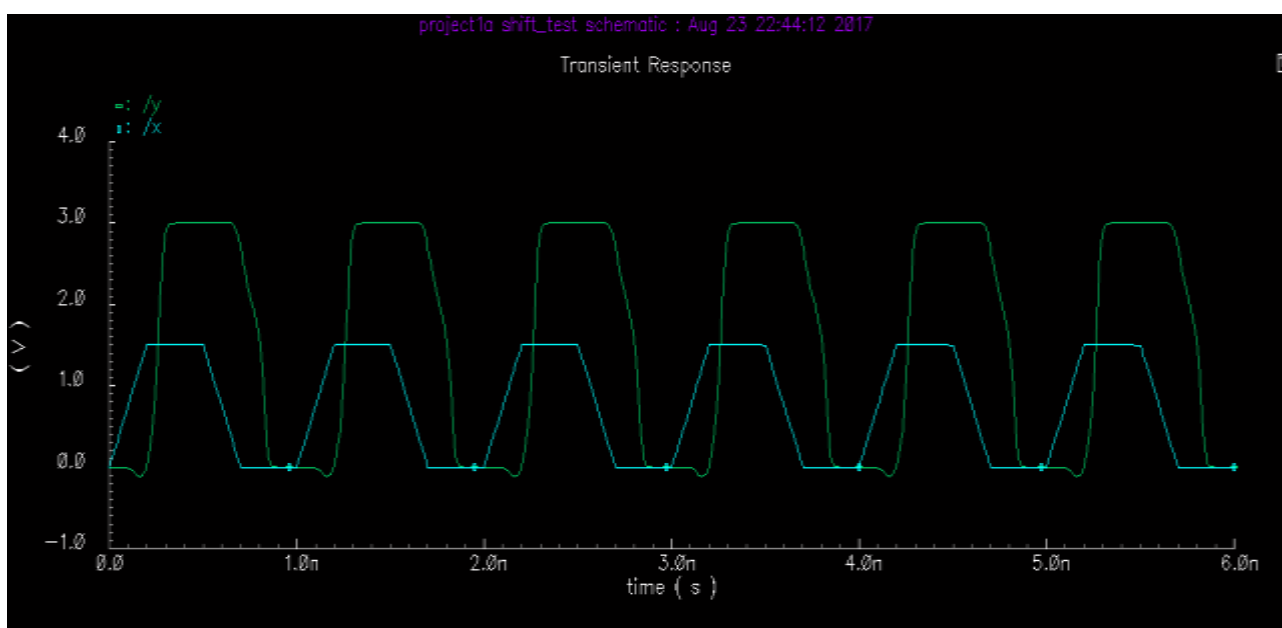


Fig. 4. Simulation result of conventional voltage level shifter

The level shifter with semi-static current mirror shown in Fig. 1 (b) is implemented in Cadence tool and shown in Fig. 5. For the circuit in Fig. 5, V_{DDL} of 1V and V_{DDH} of 3V are applied and simulated. The simulation result is shown in Fig. 6, which shows that it can convert input voltage of 1V to 3V at the output. The power consumption of voltage level shifter given

in Fig.1(b) is reduced and is lower than that of Fig.1(a). The conventional voltage level shifter (Fig.1(a)) can convert input voltages from 1.5V; it cannot convert input voltage below 1.5V. This is overcome by the level shifter in Fig. 1(b) which can convert input voltage of lower than 1.5V.

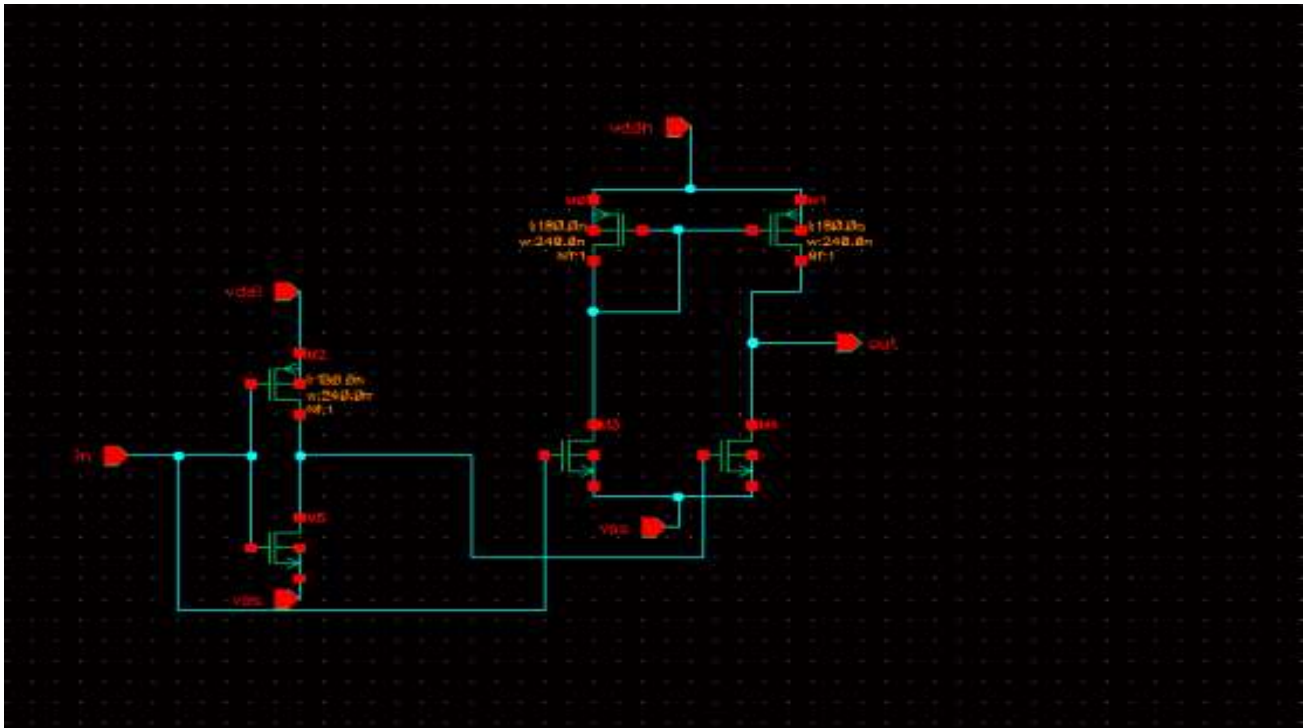


Fig. 5. Implementation of schematic of level shifter with current mirror

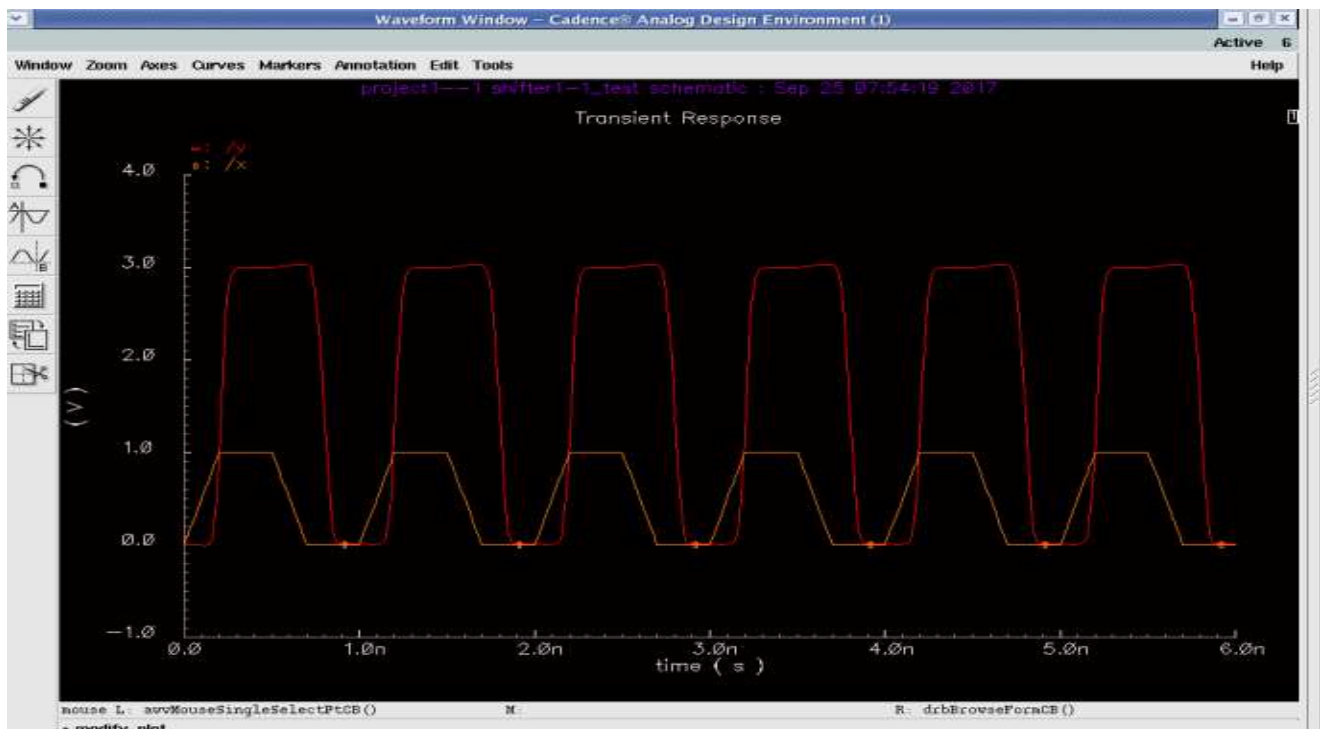


Fig. 6. Simulation results of voltage level shifter with a semi-static current mirror

The implementation of schematic of proposed level shifter is shown in Fig.7. The proposed level shifter can be able to convert extremely low input voltages also and its simulation is shown in Fig. 8. In the proposed

level shifter, V_{DDL} value is 0.8V and V_{DDH} value is 3V. The simulation of proposed level shifter shows that the circuit is capable of converting even low input voltage of 0.8V to high output voltage of 3V which is shown in Fig. 8.

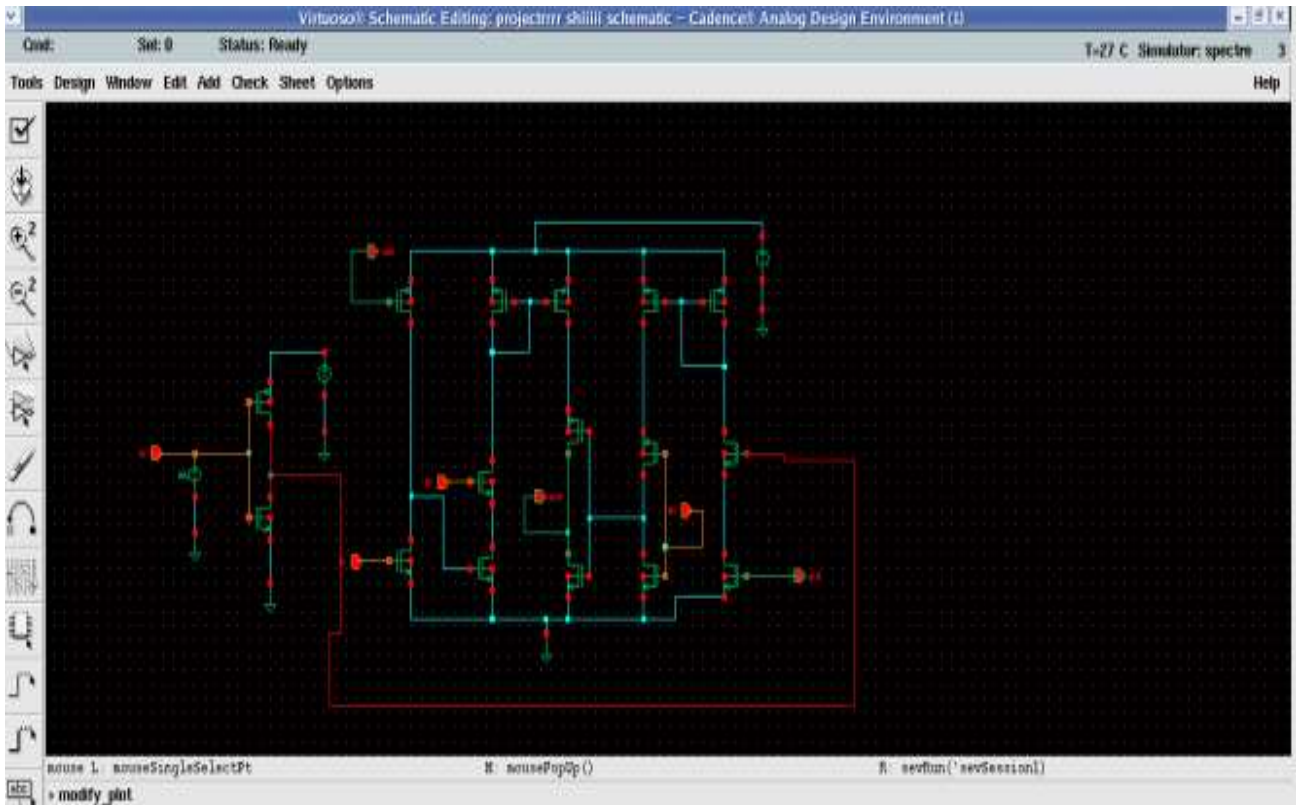


Fig. 7. Implementation of schematic of proposed level shifter

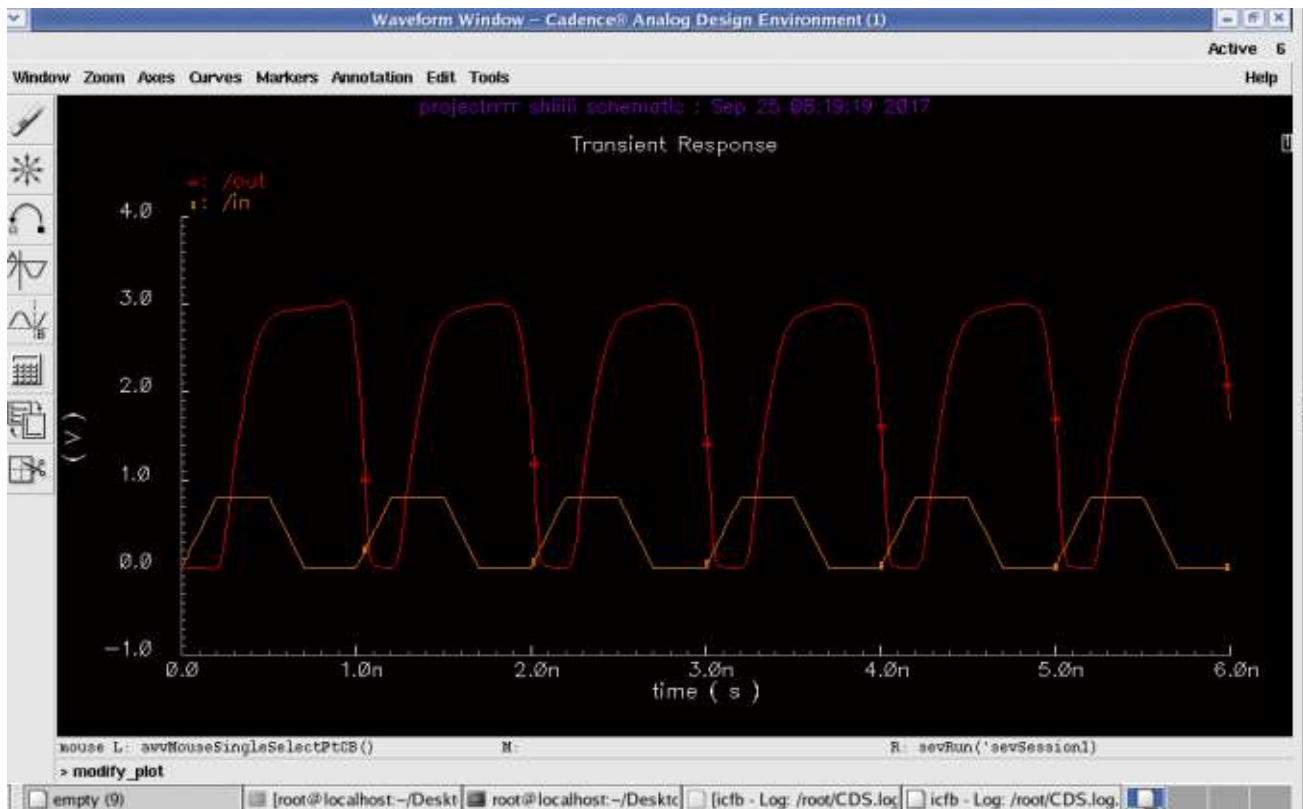


Fig. 8. Simulation result of proposed level shifter

Also when the strength, i.e., width/length value is varied for the pull-down and pull-up transistors, the power consumption is reduced further compared to the previous work and the conversion range is significantly increased. The schematic and output are shown in Fig. 9 and Fig. 10 respectively. In the proposed level

shifter, V_{DDL} value is 0.7V and V_{DDH} value is 4V. The simulation of above circuit shows that the circuit is capable of converting even low input voltage of 0.7V to high output voltage of 4V by modifying width of MOS transistors which is shown in Fig. 10. The power consumption is reduced to 1.9314 μ W.

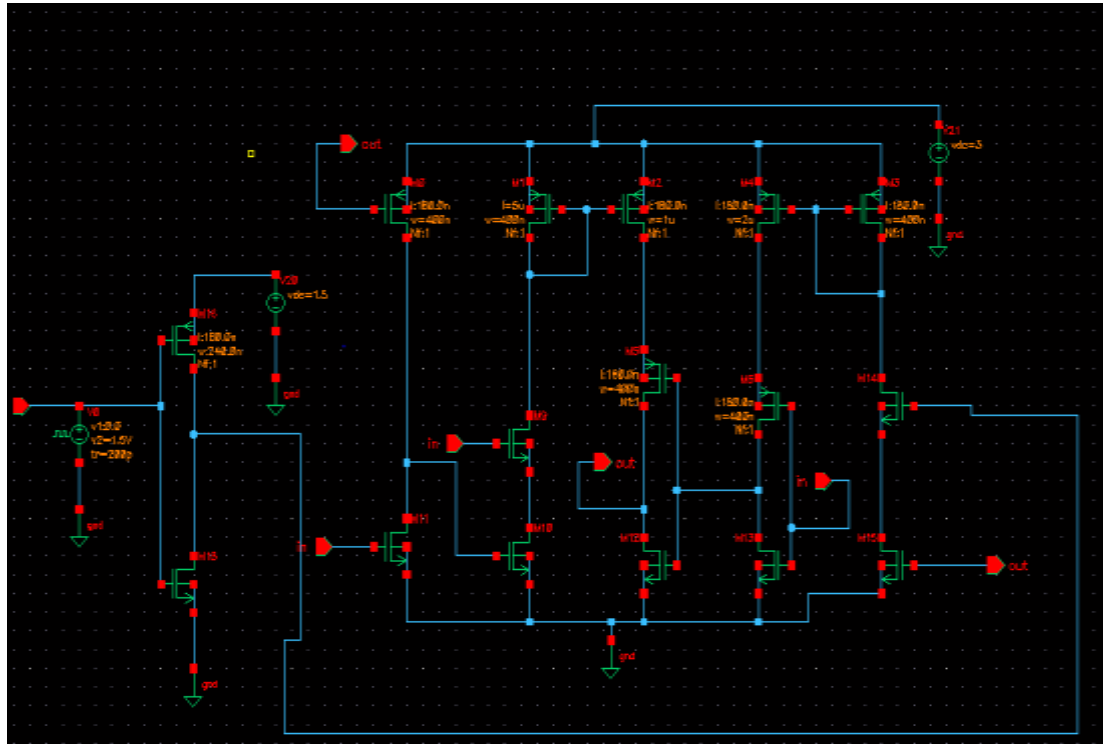


Fig. 9. Schematic of modified proposed level shifter

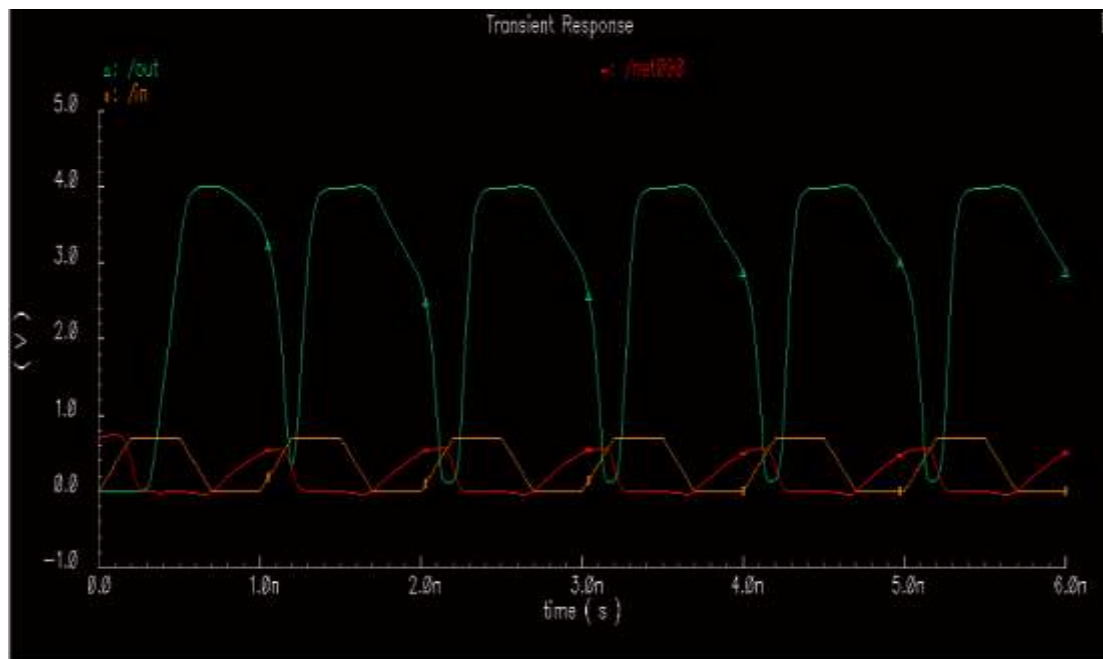


Fig. 10. Simulation result of modified proposed level shifter

The table 1 shows the comparison of power consumption of the conventional level shifters and the proposed voltage level shifter.

Table 1 summarizes the power consumption of the structures shown in Fig. 1(a), 1(b) and Fig. 2. The power consumption of the modified

proposed level shifter is reduced and is lower than the conventional level shifters. Also, the proposed level shifter can convert even extremely low level of input voltages compared to the conventional ones.

Table 1. Comparison of simulation results of the conventional and proposed level shifters

Type	VDDL	VDDH	V_{in}	V_{out}	Power for VDDL=1.5V
Fig.1(a)	1.5V	3V	1.5V	3V	453.543 μ W
Fig.1(b)	1V	3V	1V	3V	63.0609 μ W
Fig. 2	0.8V	3V	3V	3V	8.7198 μ W
Fig. 9	0.7V	3V	3V	3V	1.9314 μ W

Conclusions

An efficient and low-power voltage level-shifter design was proposed. This proposed shifter can convert extremely low level of input voltages. The power consumption of the proposed circuit is also reduced significantly. The simulation and experimental results show that the proposed level shifter is efficient compared to the other existing level shifters.

Conflicts of interest

Authors declare no conflict of interest.

References

- [1] Wang A, Chandrakasan AP. A 180-nm subthreshold FFT processor using a minimum energy design methodology. *IEEE J Solid-State Circuits*. 2005;40:310-19.
- [2] Usami K, Igarashi M, Minami F, Ishikawa T, Kanzawa M, Ichida M, Nogami K. Automated low-power technique exploiting multiple supply voltages applied to a media processor. *IEEE J Solid-State Circuits*. 1998;33:463-72.
- [3] Zhang D, Bhide A, Alvandpour A. A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13- μ m CMOS for medical implant devices. *IEEE J Solid-State Circuits*. 2012;47:1585-93.
- [4] Corsonello P, Perri S, Frustaci F. Exploring well configurations for voltage level converter design in 28 nm UTBB FDSOI technology. *Proc. IEEE Int. Conf. Comput. Design (ICCD)*. 2015; 499-504.
- [5] Lütkeemeier S and Ruckert U. A subthreshold to above-threshold level shifter comprising a Wilson current mirror. *IEEE Trans Circuits Syst II: Exp Briefs*. 2010;57:721-24.
- [6] Luo S.-C., Huang C.-J., and Chu Y.-H. A wide-range level shifter using a modified Wilson current mirror hybrid buffer. *IEEE Trans Circuits Syst I: Reg Papers*. 2014;61:1656-65.
- [7] Lanuzza M, Corsonello P, and Perri S. Fast and wide range voltage conversion in multisupply voltage designs. *IEEE Trans. Very Large Scale Integr Syst*. 2015; 23:388-91.
- [8] Osaki Y, Hirose T, Kuroki N, Numa M. A low-power level shifter with logic error correction for extremely low-voltage digital CMOS LSIs. *IEEE J Solid-State Circuits*. 2012;47:1776-83.
- [9] Hosseini SR, Saberi M, Lotfi R. A low-power subthreshold to above-threshold voltage level shifter. *IEEE Trans. Circuits Syst II: Exp Briefs*. 2014; 61:753-57.
- [10] Kwong J, Ramadas YK, Verma N, Chandrakasan AP. A 65 nm sub-V_t microcontroller with integrated SRAM and switchedcapacitor DC-DC converter. *IEEE J Solid-State Circuits*. 2009;44:115-26.
- [11] Chavan A, Mac Donald E. Ultra low voltage level shifters to interface sub and super threshold reconfigurable logic cells. *Proc IEEE Aerosp Conf*. 2008;1-6.
- [12] Hasanbegovic A, Aunet S. Low-power subthreshold to above threshold level shifter in 90 nm process. *Proc NORCHIP Conf*. 2009;1-4.
- [13] Wen L, Cheng X, Tian S, Wen H, and Zeng X. Subthreshold Level Shifter With Self-Controlled Current Limiter by Detecting Output Error. *IEEE Trans Circuits and Syst II: Exp Briefs*. 2016;63:346-50.
- [14] Maghsoudloo E, Rezaei M, Sawan M, Gosselin B. A High-Speed and Ultra Low-Power Subthreshold Signal Level Shifter. *IEEE Trans on Circuits and Syst. I: Reg Papers*. 2017;64:1164-72.
- [15] Lanuzza M, Crupi F, Rao S, Rose RD, Strangio S, Iannaccone G. An Ultralow-Voltage Energy-Efficient Level Shifter. *IEEE Trans Circuits and Syst II: Exp Briefs*. 2017;64:61-5.
