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Research Article

Design of Area Efficient Reversible Circuits using Quantum Dot Cellular Automata

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Abstract

Reversible logic has presented itself as a growing Ttechnology which plays an imperative role in quantum computing. Reversible logic has received great attention in the recent years due to their ability to reduce the area which is the main requirement in VLSI Design. The aim of the project is to design Area Efficient Reversible circuits using QCA Technology. It minimizes the power and delay. The design of digital circuits in QCA poses novel implementation strategies and methodologies are highly desirable. This reversible gates which are applicable in Nanotechnology, Quantum computing, Low power CMOS, Optical computing. QCAD Designer 2.0.3 tool is used for the implementation of QCA based Reversible Circuits. QCA design proves improvement in cell count and area.

Keywords: Quantum Dot cellular Automata; Quantum computing; Reversible Circuits; Majority Gate.

Introduction

CMOS technology has some challenging problems in scaling and energy power consumption. So that nanotechnology is used. But in nanotechnology energy dissipation is the most significant hurdle. We can make energy dissipation ideally zero, when using Reversible computation [1]. In Reversible computation number of input is equal to number of output. QCA device performs computation and carry information. Unique feature of QCA is logic values are represented using position of electrons not like voltage level in CMOS. The proposed circuits are constructed using Reversible gates using QCA in QCA Designer [2].

A novel approach to designing efficient QCA-based circuits based on Boolean expressions achieved from reconfiguration of five-input and three-input majority gates [3]. Nanotechnology is the alternative solution to these problems. International Roadmap for Semiconductor (ITRS) accounts several possible alternatives. Quantum dot cellular automata (QCA) can be one of these alternatives. QCA provides a new technique to perform computation and carry information [4]. It is easy to observe and controls the reversible circuits, due to objective properties between inputs and outputs [2]. The proposed decoder is designed using reversible QCA1 gate. QCA1 gate can function as AND-gate as well as OR-gate [5].

The multiplexer is a combinational circuit which permits picking one output amid numerous inputs. It transfers one of the inputs to the output at a time, so it is also known as Data selector. This type of operation facilitates to share one costly device for more than one application in a system. Due to its abundant use, it has become necessary to implement a multiplexer circuit which is area efficient which results in the reduction of the cost of designing [6]. Landauer demonstrated in the early 1960s, irreversible hardware computation results in energy dissipation due to the information loss, regardless of its realization technique. Landauer has shown that for irreversible logic computations, each bit of information lost generates $kT\ln(2)$ joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which the computation is performed [7].

The basic elements in QCA are cells; each cell is composed of two mobile electrons that are located in opposite corners according to columbic energy, resulting in two possible polarizations ($P = +1$, $P = -1$) [7]. A cost effective realization of 2: I multiplexer is introduced to outperform the efficiency of existing designs [8]. The most impressive

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function of reversible logic lies in quantum computing and it can be implemented through quantum dot cellular automata [9]. Normally we simulate verilog coding in XILINX ISE and simulated the waveforms. Area requirements analysed using Quartus II software. It takes area size in um^2. The coding may be in gate level, Behavioral level, or structural level.

Proposed work

Mostly the system architecture uses AND, OR and NOT gate for circuit design. It can be driven from 3 input majority gate. The 3 input majority gate has 3 inputs and 1 output and polarization states. It is shown in figure 1. The AND, OR and NOT driven from 3 input majority gates. It can be easily constructed. Logic function of majority gate is Y=AB+BC+AC.

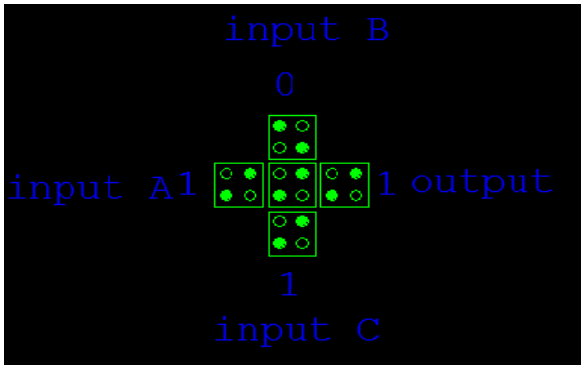

Figure 1. 3-input Majority Gate

AND gate design

AND gate is implemented by setting one of the value is equal to logic "0". It is shown in figure 2. It is given as AND=AB+B(0)+A(0)=AB.

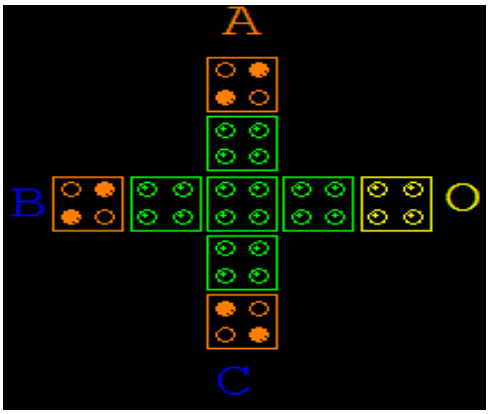

Figure 2. AND Gate Design

OR gate design

OR gate is implemented by setting one of the value is equal to logic "1". It is shown in figure 3. It is given by OR=AB+B(1)+A(1)=A+B.

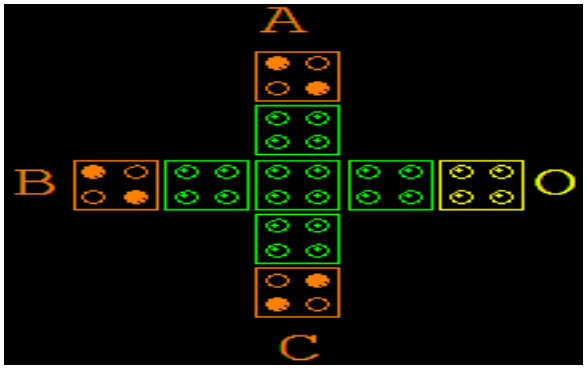

Figure 3. OR gate design

Proposed 2:1 Reversible Multiplexer

The proposed 2:1 multiplexer has two inputs 'a' and 'b', one select line sel and single output y. If select line sel=O, input 'a' is selected, and when sel=1, input 'b' performs at the output. The majority voter illustration of the function is as followed. The truth table for 2:1 Multiplexer is given in table 1.

Table 1. Truth Table for 2:1 Multiplexer

Sel0	Sel1	output
0	0	D
0	1	C
1	0	B
1	1	A

Y=MV(MV(sel',a,0),MV(sel,b,0),1)=a.sel'+b.sel (1)

The equation (1) is constructed using 2 AND and OR gates using QCA wire connection. It is shown in figure 4.

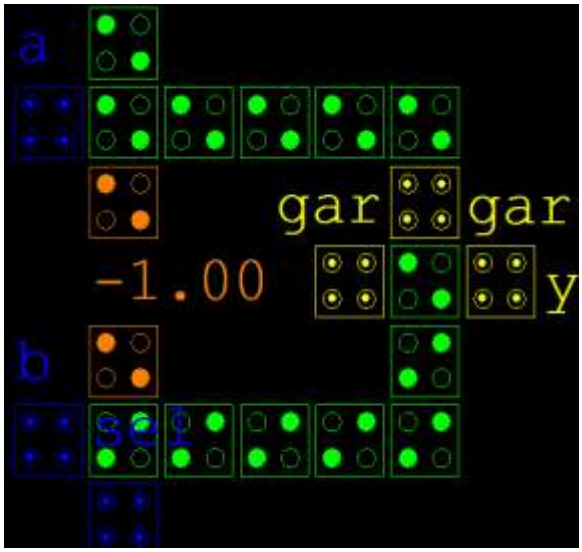

Figure 4. Proposed 2:1 Multiplexer QCA design

Proposed 4:1 Reversible Multiplexer Design

It consists of two select inputs and depending upon these select inputs output is selected. Output function is derived as given in equation (2).

F=Sel0".Sel1".a+Sel0.Sel1".b+Sel0".Sel1.c+Sel 0.Sel1.d (2)

The 4:1 Multiplexer designed using cascading of 2 2:1 Multiplexer. It is shown in figure 5. The proposed 4:1 Multiplexer QCA design uses 60 cells. It includes 6 Majority gates connected through Quantum wires. It cascades two 2:1 Multiplexer QCA design. It is shown in figure 5. 4:1 Reversible Multiplexer uses 4 inputs, 2 selection inputs and 1 output.

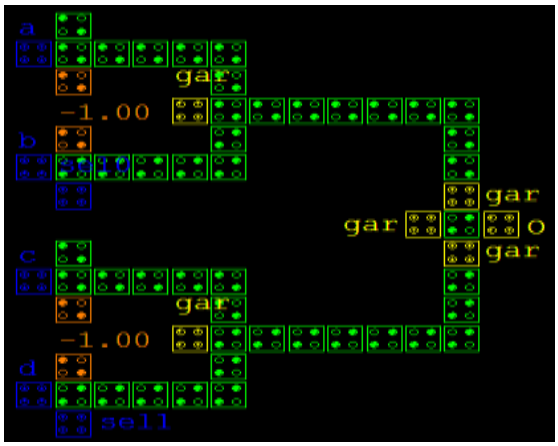

Figure 5: Proposed 4:1 Multiplexer QCA design

Proposed 1:2 Reversible Decoder Design

QCA1 reversible gate is used to design Reversible Decoder. QCA1 gate can function as 1-to-2 decoder, if the input "a" of QCA1 gate is fixed to logic '0'. In this case the inputs "b" and "c" must be considered as enable input(En) and general input(W0) of the decoder, respectively. The output y1 will be EnW0 and the output y0 will be EnW0. The third output is considered as garbage (Gar) output. The schematic diagram is shown in figure 6.

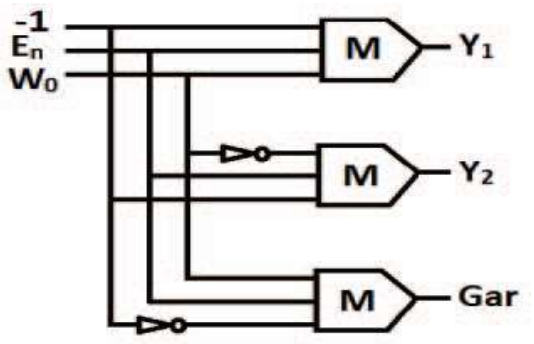

Figure 6. Proposed 1:2 Reversible Decoder schematic diagram

The output equation of majority gate is given in equation (3).

Y1=M (0, En, W0)
Y2=M (0, En, W0') (3)

Proposed 1:2 decoder uses 3 majority gates and 2 inverters. It is shown in figure 7.

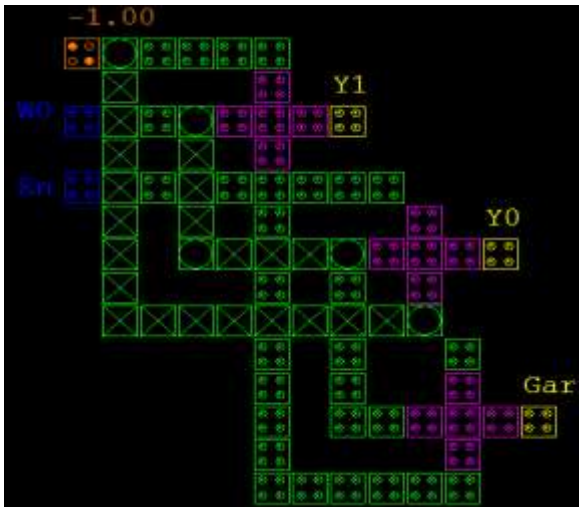

Figure 7: Proposed 1:2 Reversible Decoder QCA design

Proposed 2:4 Reversible Decoder

Reversible 2:4 decoder can be made by cascading three Reversible 1:2 decoders. The inputs En and W0 are applied to first 1:2 decoder circuits. The input bit W1 is applied to second and third 1:2 decoder circuits. The two outputs of first 1:2 decoder circuit are used as an input to second and third 1:2 decoder respectively. The proposed design has only three garbage outputs. Its schematic diagram is shown in figure 8. The majority gate based expression written as equation (4).

Y0= M (0, M (0, En, W0'), W1')
Y1= M (0, M (0, En, W0'), W1)
Y2= M (0, M (0, En, W0), W1')
Y3= M (0, M (0, En, W0), W1) (4)

The QCA layout of Reversible 2:4 decoder requires nine majority gates and six inverters. It is shown in figure 9.

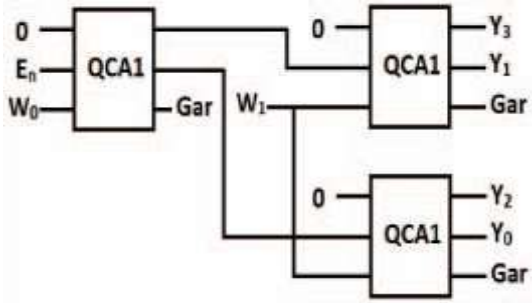

Figure 8. Proposed 2:4 Reversible Decoder schematic diagram

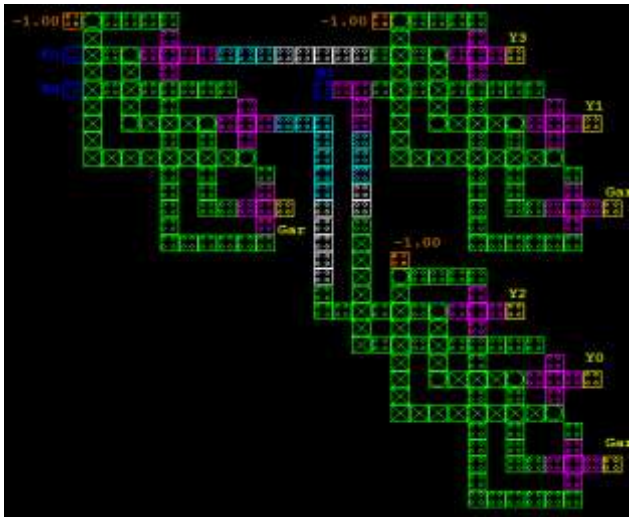

Figure 9. Proposed 2:4 Reversible Decoder QCA design

Results and Discussion

The proposed 2:1 multiplexer QCA design uses 21 cells. It includes 3 Majority gates and Quantum wires. It was shown in figure 4. AND gate and OR gate constructed from Majority gates by giving one of the input as "0" or "1". The 2 AND gates are connected to OR gate using Quantum wires. The Quantum wire work is to propagate without any information loss. When input sel=0, Output y=logic value of "a". When input sel=1, Output y=logic value of "b". The outputs are verified as shown in figure 10.

The output function is verified from figure 11. When s0 and s1 is in "0" condition, the output O selects "a" input. If s0=0, s1=1, output O=logic value of "b", s0=1, s1=0, output O=logic value of "c" and s0=1, s1=1, output O=logic value of "d". Inputs -En and W0, Outputs – y1 and y2, when input W0 is "0", the output Y0 will be "1" with respect to enable input is on condition. If W0 is "1", the output Y1 will be "1". The output is verified from figure 12. Inputs-En, W0, W1, Outputs-y0, y1, y2, y3, when inputs a=0, b=0, Output y0=1, inputs a=0, b=1, Output y1=1, inputs a=1, b=0, Output y2=1, inputs a=1,b=1, Output y3=1. The output is verified from figure 13.

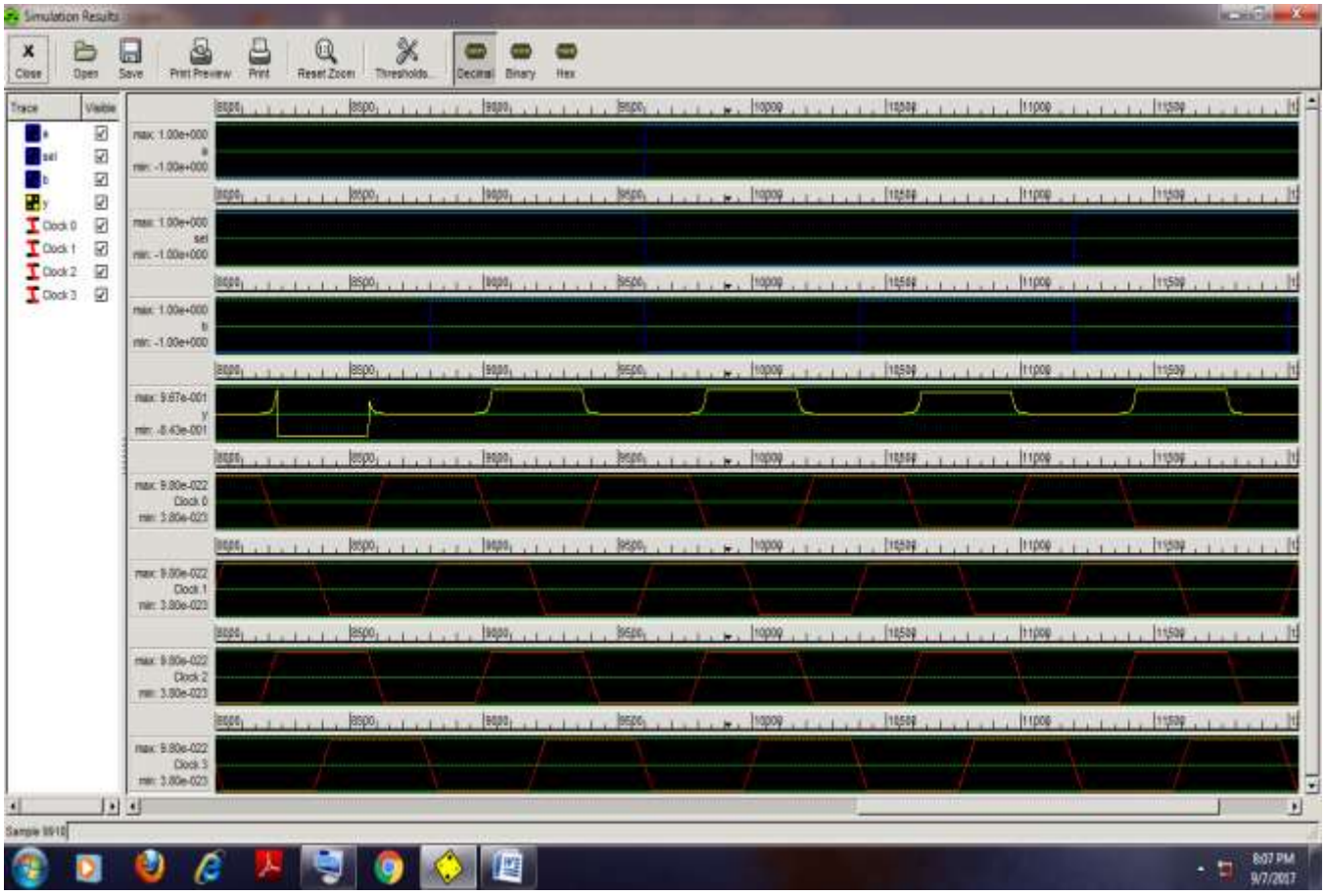

Figure 10. Result of 2:1 Reversible Multiplexer

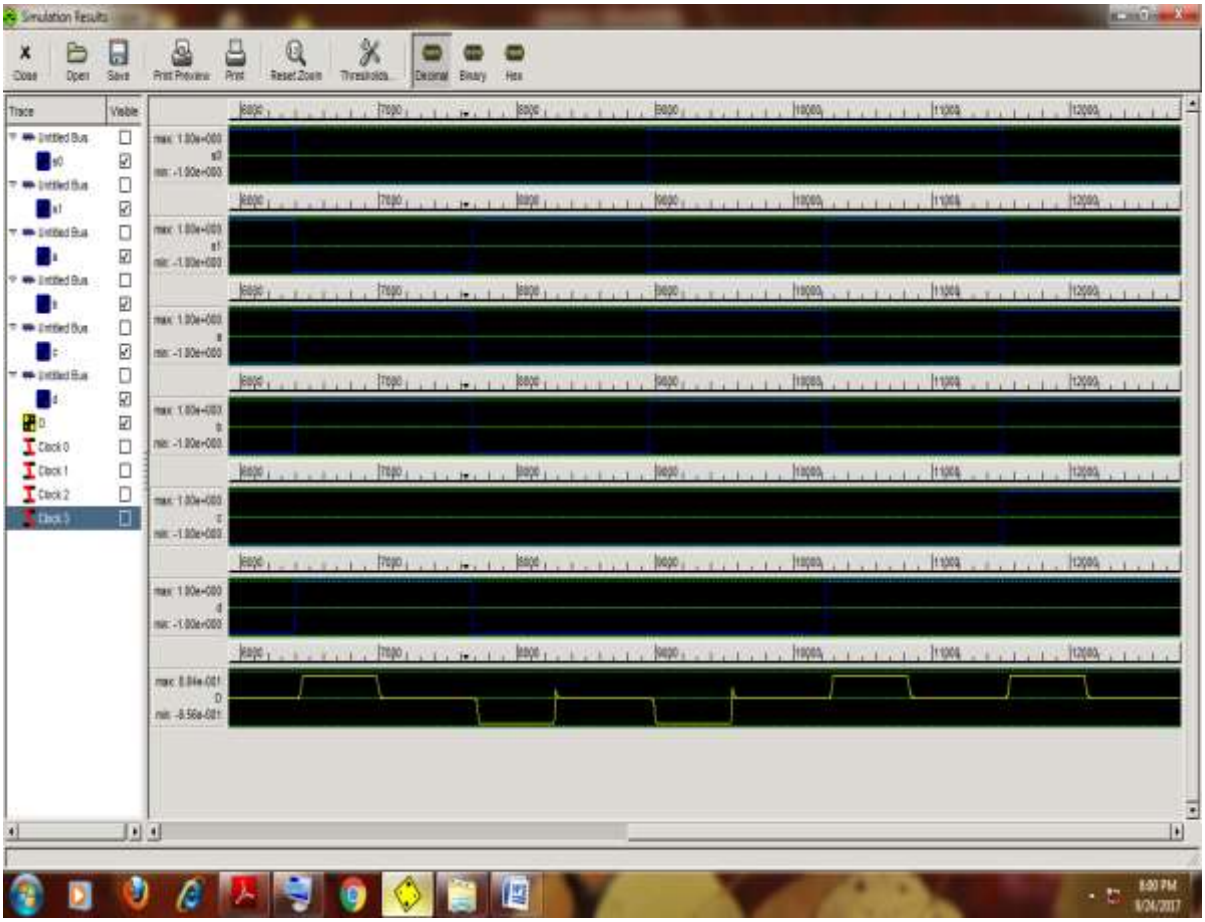

Figure 11. Result of 4:1 Reversible Multiplexer

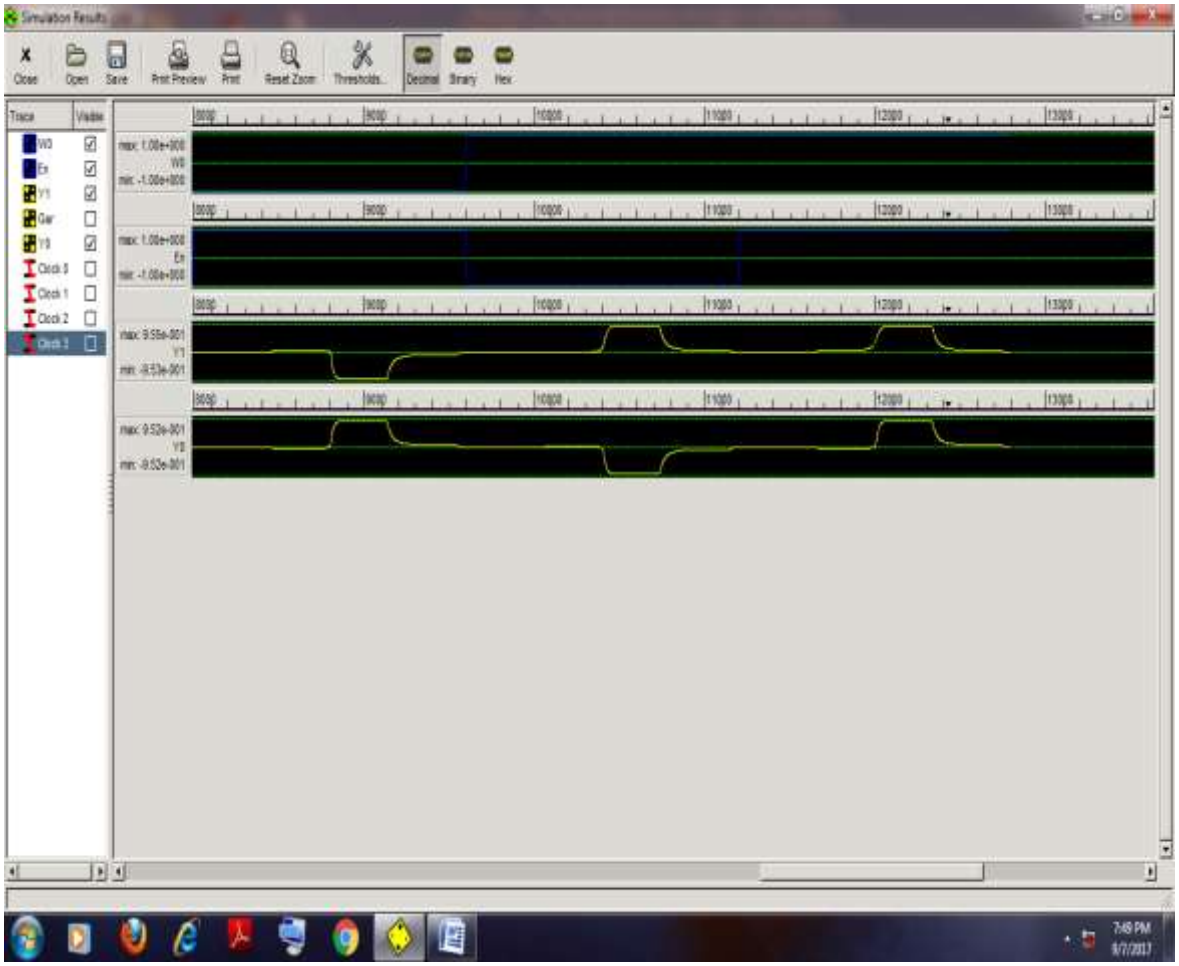

Figure 12. Result of 1:2 Reversible decoder

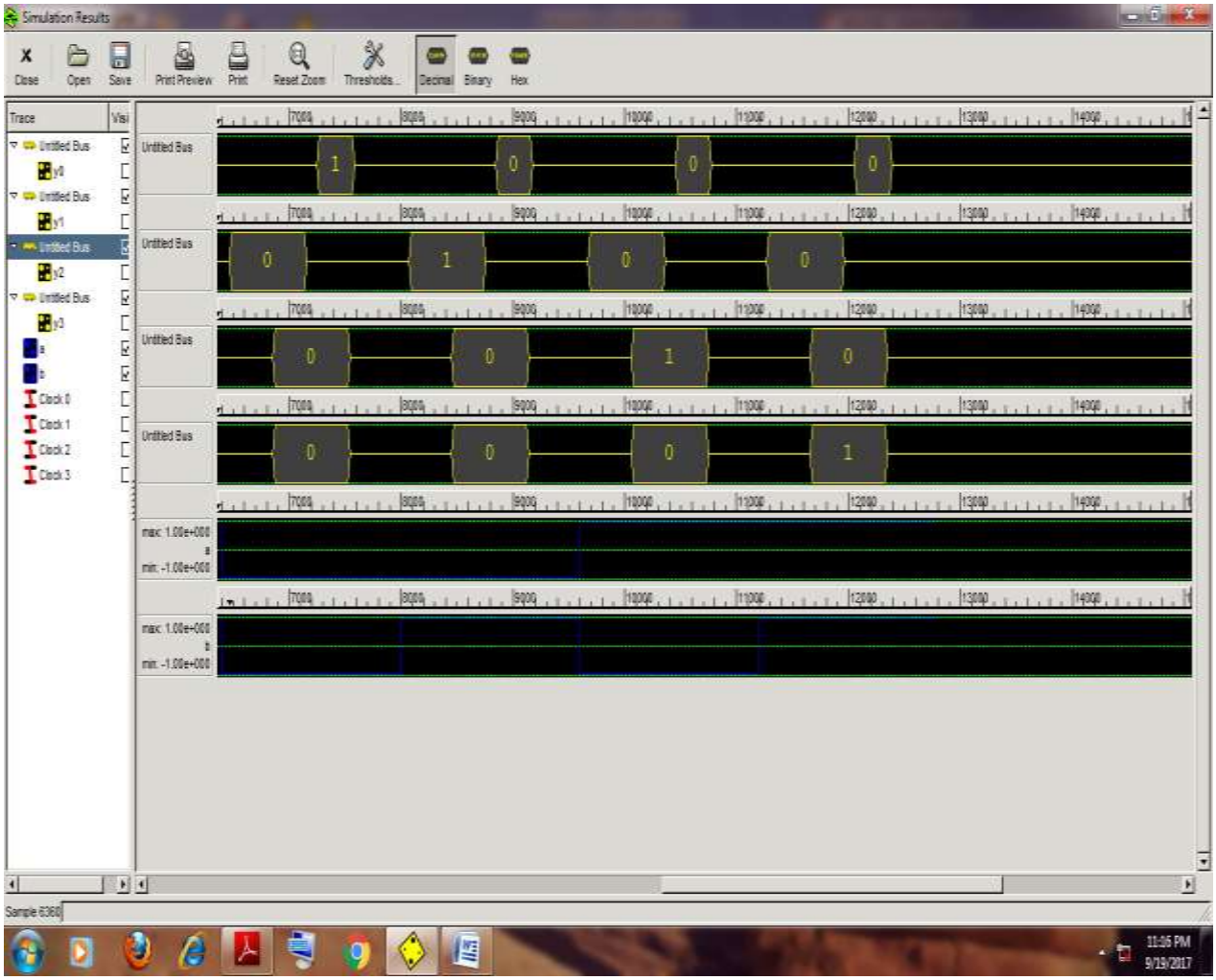

Figure 13. Result of 2:4 Reversible decoder

Table 2. Area estimation of reversible circuits

Circuit Design		Area, um^2
1:2 DECODER	Conventional Circuit	0.08
	Proposed Reversible Circuit	82474
2:4 DECODER	Conventional Circuit	0.45
	Proposed Reversible Circuit	376259
2:1 MULTIPLEXER	Conventional Circuit	0.08
	Proposed Reversible Circuit	19044
4:1 MULTIPLEXER	Conventional Circuit	0.23
	Proposed Reversible Circuit	78459.7

Conclusions

The project paper demonstrated QCA based novel nano-scale reversible circuits. The new layout of QCA is denser than existing circuits. It shows that QCA is alternative platform to CMOS, for implementing Reversible circuits. Truth table based comparison of simulation results established the design accuracy. The proposed circuits can be used to design reversible architecture for nano-communication systems. In future work is to design a Reversible Processor using QCA to reduce area.

Conflicts of interest

Authors declare no conflict of interest.

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