

Research Article

An Efficient Approach for Test Pattern Generation in Scan Based BIST

R. Kavitha, R. Vishnupriya*

Department of Electronics and Communication Engineering, Arasu Engineering College,
Kumbakonam – 612501. India.

*Corresponding author's e-mail: kavitharamesh1995@gmail.com

Abstract

A new low-power (LP) scan-based BIST technique is proposed based on weighted pseudo random test pattern generation and reseeding. This project describes a LP (low power) Weighted pseudo random test pattern generator (PRPG) which has the capacity to produce the pseudo random test pattern generator with reseeding. LP (low- power) reseeding techniques are used to create a feedback for high accuracy and also cover a number of test vectors. In both techniques, only a small number of flip flops can activate. The gating technique is used to disable unwanted flipflops. Due to low switching activity, power will be minimized. The LFSR is used to implement the test pattern for detecting faults. DFT architecture is used to implement the deterministic BIST for reduced test vectors. The design has been coded in verilog. The simulation results have been viewed by Modelsim software and Quartus II software. The obtained simulation results can be used for industrial applications.

Keywords: Built In Self Test; Pseudo Random Test Pattern Generator; Linear Feedback Shift Register; Design For Testability.

Introduction

Modern day computers are smaller, faster, and cheaper and more power efficient. With laptops, tablets and smart phone flooding the markets, the progress every second is obvious. The new domain of computing was ushered in by multiple advancements in electronic miniaturization and the semiconductor transistor by Bardeen in 1947-48, and then the Bipolar Transistor by Shockley in 1949. By mid-1980, the transistor count on a single chip exceeded 1000 and hence came the age of Very Large Scale Integration (VLSI), which is large scale integration with a single chip of size as small as 50 millimeters square having more than a million transistors and circuits in it. In VLSI, testing is an essential part of designing a circuit. It is used to compute defects in all circuits. The reliable VLSI circuits depend strongly on testing to eliminate various faults caused by the manufacturing process [1]. The basic defects are misalignment, holes, and physical failures, charge injection problems [2]. These defects are determined by parametric testing or logical testing. If small number of test vectors is used, each node of circuit proves a fault free. The good observability and controllability is used to

reduce a test vectors. The present work is proposed a weighted pseudo random test pattern generation and reseeding techniques based on low power scan based Built in self-test (BIST). Scan is used to testing sequential circuits in efficient manner. Low power design is the major design objective which is widely used for communication, signal processing and IC fabrication technology. Low power testing may be measured with the switching activity of the scan cells [3].

BIST is the capability of the circuit to test itself. BIST techniques are used to find the faults in a circuit design and also reduced the difficulty in VLSI testing. But the power consumed during test mode operation is often much higher than normal mode operation because of the high switching activity in the nodes of the CUT during test mode which causes the excessive power dissipation in the circuit. So, the present work is strongly focused on reducing the switching activity and also to develop an efficient algorithm in terms of area and low power and also reduce the test time. Furthermore, the power dissipation of scan-based built-in self-test (BIST) is much higher than power dissipation in deterministic scan testing due to excessive switching activities

caused by random patterns [4]. Recent methods [5,6] are low power test compression and launch on shift whose test generator is pseudo random test pattern generator. It's aim at reducing a switching activity and power. But, these methods are achieved a power dissipation due to more flipflops used for scanning process. To overcome these problems, weighted pseudo random test pattern generation with reseeding is proposed.

In the present work, it is proposed a new LP scan based BIST, which supports a LP weighted PRPG, LP Reseeding, LP Deterministic BIST. Design for testability, DFT must be a central element of any design process these days. The only way that tolerable testing can be obtained by employing design for test. The DFT Architecture which is used to implement the deterministic BIST [5]. We present the major contribution of this paper in the following. A new LP weighted pseudorandom test pattern generator using weighted test-enable signals is proposed using gating techniques. A new LP deterministic BIST scheme is proposed to encode the deterministic test patterns for random pattern- resistant faults. Only a part of flip flops are activated in each cycle of the whole process of deterministic BIST. A new algorithm is proposed to the number of extra variables injected into the linear-feedback shift register (LFSR) that encode all deterministic patterns. A new LP Reseeding scheme, which is creates a feedback for high accuracy and it can cover a number of test vectors which is allows a small number of flipflops for scanning process.

In Previous methods, [7] the LFSR is commonly used in the test pattern generators (TPGs) and output response analyzers. It is used to generate a desired test pattern for given test vectors. A major drawback of these architectures is that the pseudorandom patterns generated by the LFSR lead to significantly high switching activities in the CUT which can cause excessive power dissipation. It can also damage the circuit and reduce product yield and lifetime. Several low-power approaches have been developed based on scan-based BIST to reduce the switching activities but it cannot consider about fault coverage. Some methods have high power dissipation due to excessive switching activity.

A novel BIST scheme that inserts multiple capture cycles after scan shift cycles during a test cycle. As a result, fault coverage only

improved. This paper consider about only scan based BIST and pseudo random test pattern generation. Proposed, a new LP scan-based BIST technique is proposed based on weighted pseudorandom test pattern generation and reseeding. DFT architecture is proposed, which supports both pseudorandom testing and deterministic BIST.

Weighted pseudo random testing schemes [1, 2, 5, 8, 10] can effectively improve fault coverage. But it does not consider a reseeding scheme. Reconfigurable scan architecture was used for the deterministic BIST scheme using the weighted test enable signal-based pseudo random test generation scheme proposed a new scan segmentation approach for more effective BIST. LP BIST approaches were proposed early proposed a distributed BIST control scheme in order to simplify the BIST execution of complex ICs. The average power was reduced and the temperature also reduced.

A new DFT scheme for launch-on-shift testing [7] was proposed which ensures that the combinational logic remains undisturbed between the interleaved capture phases, providing computer-aided-design tools with extra search space for minimizing launch-to-capture switching activity through test pattern ordering. A new adaptive low shift power pseudorandom test pattern generator [3] was presented to improve the tradeoff between test coverage loss and shift power reduction in logic BIST. Deterministic BIST scheme is proposed to encode the deterministic test patterns for random pattern- resistant faults. In our method, scan based BIST for weighted pseudo random test pattern generation and Reseeding techniques [1, 2, 7, 10-12]. The scan architecture is same both previous methods and proposed one. A main difference of both is phase shifter. In our method, phase shifter drives a multiple test vectors at a time. Thus, test time and power, area is reduced.

Proposed work

Scan-based, self-test architectures are popular because of their low impact on performance and area. These scan-based architectures are expensive because each test pattern requires a power-consuming shift operation to provide test patterns and evaluate test response .To meet specified power limits during test and avoid system destruction, it is

important to reduce power dissipation during scan shifting. In the present work, three techniques for reducing power dissipation of scan-based BIST architectures are proposed.

LP weighted pseudo random test pattern generation

DFT Architecture

Design for testability techniques [13] are design efforts specifically employed to ensure that a device is testable. DFT techniques are used to improve a circuit's controllability and observability [3]. Controllability is the ability to establish a specific signal value at each node in a circuit by setting values on the circuit's inputs. Observability, on the other hand, is the ability to determine the signal value at any node in a circuit by controlling the circuit's inputs and observing its outputs. It is used to implement the deterministic scan based BIST. In previous method, scan –forest architecture used [1, 5, 8]. In this case, the phase shifter drives a one scan chains at a time. In our method, phase shifter drives a multiple scan chains at a time. As a result, test time and switching activity will be reduced.

The general DFT Architecture for LP scan-based BIST shown in Fig. 1. The weighted scan enable signals are feed through the multiplexers for creates a weighted test pattern generation. The separate weighted enable signals are e_0, e_1, \dots, e_n . BIST controller consists of a test enable, clk, hold latch, shift cycle (B_1 to B_K) and capture cycle (A_1 to A_K). This controller is used to send a test vectors to LFSR and MUX. The test vectors are enabled for scan a flipflops by using MUX. The shadow register is used for LP Deterministic and Reseeding. The initial values kept in the LFSR are stored in the shadow register. LFSR is used to generate a test pattern for given test vectors. Each stage of the PS drives multiple scan chain instead of a single scan chain, while each stage of the PS requires a few number of XOR gates. As a result, test vectors are reduced. CUT is used to compare the LFSR pattern and after scanning pattern. These test patterns of test vectors are given to the MISR. Output response is kept in MISR. Again, this test vectors are feed to the BIST controller for detects faults.

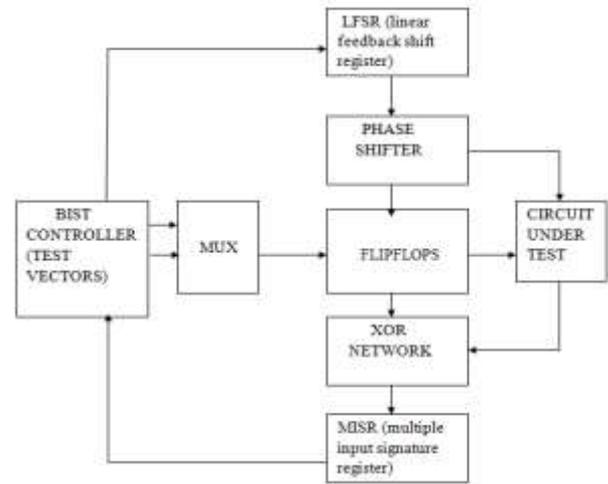


Fig. 1. General DFT architecture for LP scan-based BIST

Weighted pseudorandom test pattern generation

Our method generates an activated scan chains for test pattern generation. Test pattern generation is the process of determining the stimuli necessary to test a digital system. Pseudorandom testing, where test patterns are generated in pseudorandom manner. The cost of this type of test is considerably reduced. It deals with testing a circuit with test patterns that have many characteristics of random patterns [2, 9] but where the patterns are repeatable. It is applicable for both combinational and sequential circuits. Weighted PRPG is a one type of test pattern generation. It is used to produce a 0s and 1s on the output lines. Non-uniform distribution of 0's & 1's, improved fault coverage, using LFSR added with combinational circuits [14]. So, the present work used a weighted pseudo random TPG. Operation of test pattern is shown in Fig. 2. We generate weights of the test enable signals for all scan chains in LP DFT Architecture [1, 15]. The gating technique is used to disabled unwanted a scan chains [2, 14]. A Part of flipflops are activated in a scan process. Thus, switching activity and also power is reduced.

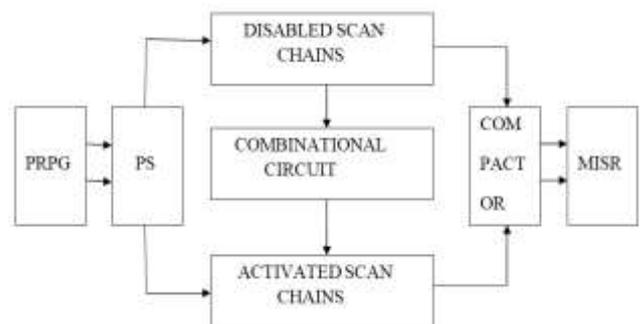


Fig. 2. Weighted pseudorandom test pattern generator for LP scan-based BIST

LP reseeding scheme

BIST reseeding [15] is used to improve fault coverage by reinitializing the PRPG to generate deterministic test patterns that target specific faults. Most of the previous work done on reseeding is based on storing the test vectors in the ATE (External Testing). Our techniques are LP built-in reseeding. Due to no storage of test vectors, memory requirement is less. The seeds (Test vectors) are encoded in circuitry on the product chip. In reseeding, the test storage are proportional to the number of test vectors. This dissertation presents an algorithm [13] for ordering the seeds in order to reduce the number of seeds needed to produce a set of deterministic test patterns.

LP deterministic BIST with extra variable injection

The present work proposed a LP deterministic BIST scheme [11, 14] with reseeding. The deterministic test vectors [3] for the random-pattern resistant faults are ordered according to the number of care bits. Our method partitions all scan chains into multiple subsets, while only one subset of scan trees is activated at

any clock cycle. The gating logic controls the whole test application process. The first deterministic test vector is shifted into all scan trees as follows. The seed is first shifted into the LFSR [11, 12]. The extra variables with calculated values are injected into the LFSR when the seed is applied to the first subset of activated scan trees. The same values on the extra inputs are delivered after the same seed is loaded to the LFSR again for the second subset of activated scan trees. This process continues until all scan trees have received the test vector.

Results and discussion

The approach of scan architecture is validated by four modes of operation. The operations are (i) Idle mode (ii) BIST write mode (iii) Pattern check mode, and (iv) BIST valid mode.

Idle mode

Before the Idle mode, the address of write, read and data generation does not produced. Assigning idle mode of clock as 1 and output of test vectors is generated from each clock cycle. Result shows that unique test pattern is calculated (Fig. 3).

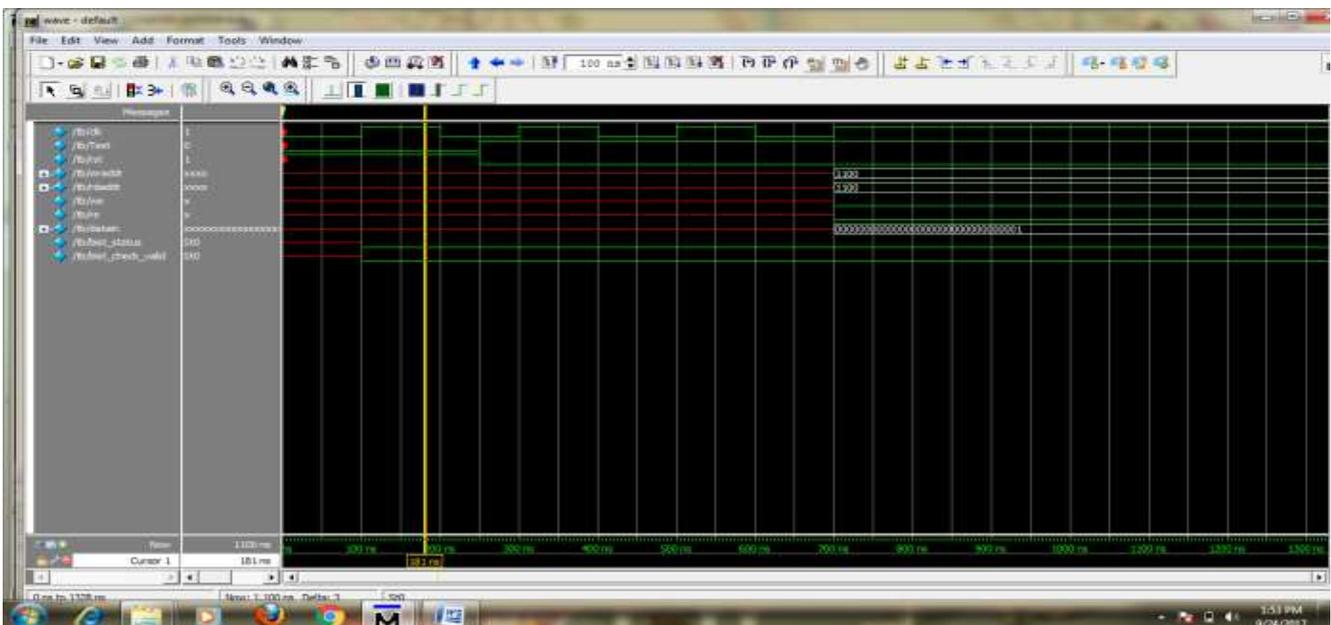


Fig. 3. Test pattern for idle mode

In this wave form, three states are used such as clock, reset, and test. Depending on these three states, we can detect faults in a circuit. 32 bit sequence of test vectors and 4 bit address used and this vectors applied to scan chain to reduced area over head and power distribution and run time. At initial condition, clock and reset is enable, write and read state is disable. If it is in

idle state, address of read, write and data generation will be zero.

BIST write mode

After idle mode, write and read state will be enabled. We have to give an address for data enable and read, write state for storing a test vectors. If BIST modes write, BIST control and

generation of test vectors are enabled. During a testing process (Fig. 4), it can achieve storage of test vectors in the content of particular address location.

Pattern check mode

In this operation, write state is disabled and read state will be enabled. As a result, 32 bit data continuously processed (Fig. 5). Extra variable

injected to a 32 bit data. That means fault is occurs.

BIST valid mode

If extra variable injected in pattern check mode, fault will be occurs. Test pattern will be checked by using comparator, the CUT act as a comparator. If CUT output is high, fault will be detected otherwise no fault is occurred in testing process (Fig. 6).

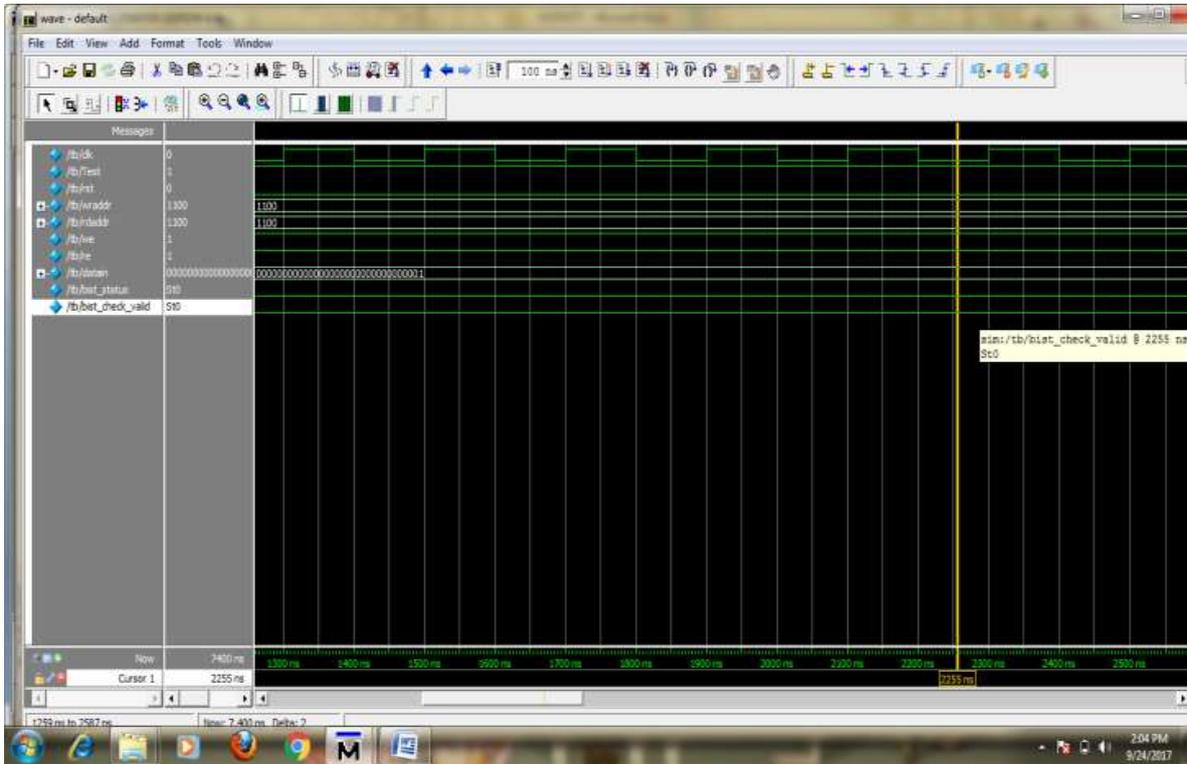


Fig. 4. Test pattern for BIST write mode

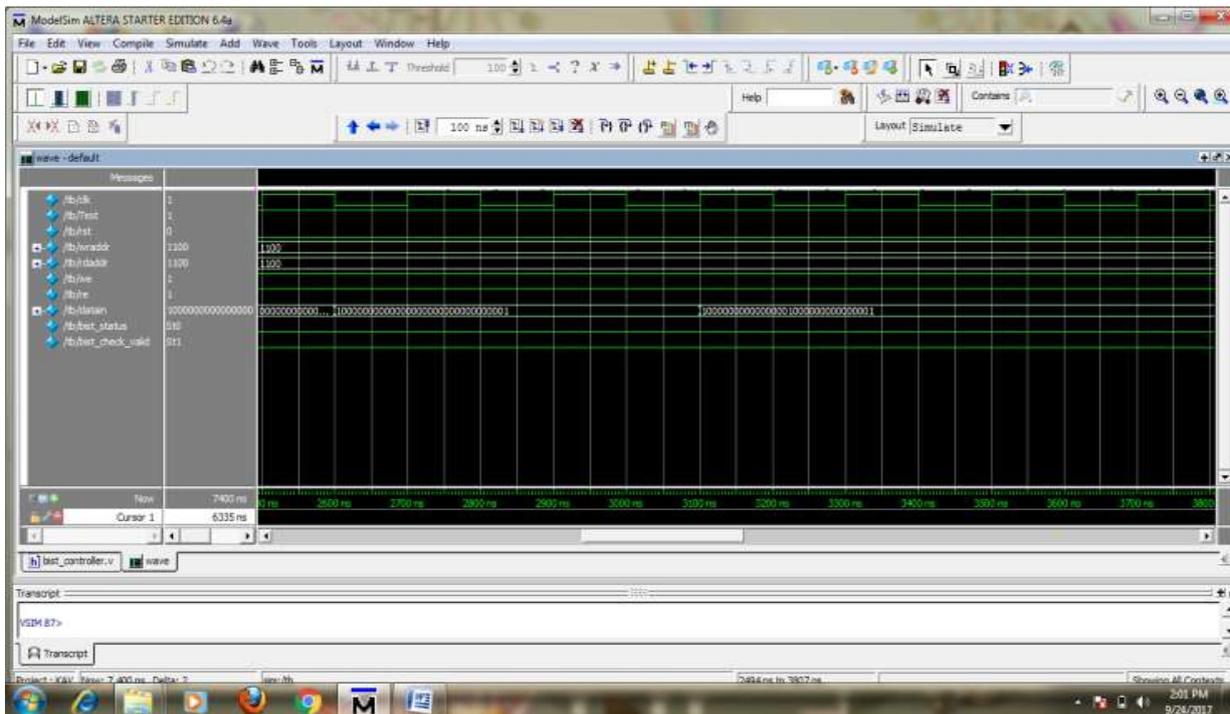


Fig. 5. Test pattern for pattern check mode

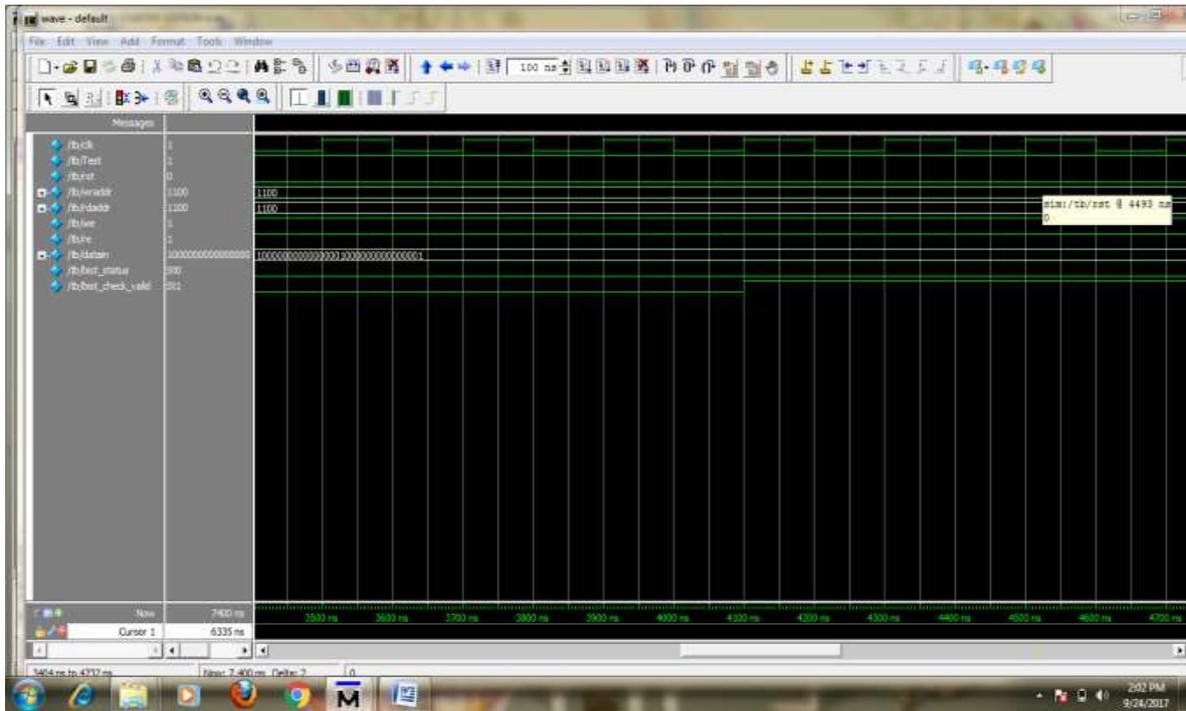


Fig. 6. Test pattern for BIST valid mode

Table 1. Power, area, test time comparison of LP weighted pseudo random test generator

Parameters	Existing	Proposed
Power	48 mw	34.47 mw
Area efficiency	45%	53%
Run time	7.032 ns	4.451 ns

The proposed design is compared with a conventional scan based test design in terms of area, power and speed. After simulation, using Quartus –II software I have analysed these three parameters for both the cases. As the numbers of flipflops are reduced in proposed design comparing to existing one, the power consumption and area are significantly reduced. From the above table shown in 4.1, we analysed that power consumption is decreased by 14 mW.

Conclusions

The BIST architecture proposed is implemented using Verilog language and tested on various faulty circuits. Then design has been synthesized on fault has been created and simulated on Modelsim software and power, area, speed has been analysed by Quartus II power analyser tool. In this study, a new LP Weighted pseudo random test pattern generation with reseeding and deterministic BIST is proposed. A new BIST design is described for saving energy both LFSR and the CUT in a random testing environment. To reduce a power, speed, area, a different set of useful test vectors is to be selected from the

random sequence, or the scan path architecture is to be radically redesigned. Experimental results have demonstrated the performance of the proposed method by comparison with a recent LP BIST method.

Conflicts of interest

Authors declare no conflict of interest.

References

- [1] Jas A, Krishna CV. Weighted pseudo random hybrid BIST. *IEEE Trans Very Large Scale Integr Syst*. 2004;12:1277–1283.
- [2] Kapur R, Patil S. A weighted random pattern test generation system. *IEEE Trans Comput Aided Des Integr Circuits Syst* 1996;15:1020–1025.
- [3] Abu-Issa S, Quigley SF. Bit-swapping LFSR and scan-chain ordering: A novel technique for peak-and average-power reduction in scan-based BIST. *IEEE Trans Comput Aided Des Integr Circuits Syst* 2009;28:755–759.
- [4] Gerstendörfer S, Wunderlich HJ. Minimized power consumption for scan-based BIST. *J Electron Test* 2010;16:203–212.
- [5] Filipek M, Mrugalski G, Mukherjee N, Dostie BN, Rajski J, Solecki J, Tyszer J. Low-power programmable PRPG with test compression capabilities. *IEEE Trans Very Large Scale Integr Syst* 2015;23:1063–1076.

- [6] Girard P, Landrault C, Pravossoudovitch S, Virazel A. High defect coverage with low-power test sequences in a BIST environment. *IEEE Des Test Comput* 2002;21:44–52.
- [7] Basturkmen NZ, Reddy SM, Pomeranz I. A low power pseudorandom BIST technique. *J Electron Test* 2003;19:637–644.
- [8] Hellebrand S, Rajski J, Tarnick S. Built-in test for circuits with scan based on reseeding of multiple polynomial linear feedback shift registers. *IEEE Trans Comput* 1995;44:223–233.
- [9] Kiefer G, Wunderlich HJ. Deterministic BIST with multiple scan chains. *J Electron Test* 1999;14:85–93.
- [10] Jee J, Touba NA. LFSR-reseeding scheme achieving low-power dissipation during test. *IEEE Trans Comput Aided Des Integr Circuits Syst*. 2007; 26:396–401.
- [11] Kim H, Kang S. Increasing encoding efficiency of LFSR reseeding-based test compression. *IEEE Trans Comput Aided Des Integr* 2006;25:913–917.
- [12] Omaña M, Rossi D. Novel approach to reduce power droop during scan-based logic BIST. *IEEE European Test Symposium*, 2016.
- [13] Nourani M, Tehranipoor M. Low-transition test pattern generation for BIST-based applications. *IEEE Trans Comput* 2008;57:303–315.
- [14] Koenemann B. LFSR-coded test patterns for scan designs. *European Test Conference*, 1999.
- [15] Rajski J, Tyszer J. Embedded deterministic test. *IEEE Trans Comput Aided Des Integr Circuits Syst* 2014;23:776–792.
