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Research Article

Design and Performance Analysis of VLSI Architecture for Inexact Speculative Adder

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Abstract

Low power and high speed design is one of the important building blocks in digital circuits. In conventional Inexact speculative adder based on x-bit adder to consume more power issues and long critical path delay. In this paper, carry look-ahead adder based design of the proposed ISA architecture which is fine grain pipelined because to increase the processing speed. Additionally this architecture has been clock gated giving rise to dynamic power reduction opportunity. Functional verification and hardware implementation of suggested Inexact Speculative Adder (ISA) is carried out on Field Programmable Gate Array (FPGA).

Keywords: Inexact speculative adder; Carry look-ahead adder; Pipelining; Field Programmable Gate Array; Clock gated.

Introduction

In electronics, an adder is a digital circuit that performs addition of binary numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic units, but also in other parts of the processors, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations. High speed adders are highly desirable in the present day scenario, though power and silicon area are equally vital [1]. Spectrum sensors used in intelligent cognitive-radio environment as well as internet of everything (IOE) devices focused on physical interfaces are largely-explored research areas in the recent time [2]. With tolerable degradation in accuracy and performance, it is feasible to conceive high-speed, low power and area efficient design using inexact and approximate circuit technique [3]. Accuracy of such circuits can be traded off to improve the power and speed by speculation. Thereby, such adders are referred as inexact speculative adder (ISA). Various optimized versions of such ISA have been reported and these works concentrated mostly on enhancing the accuracy of their results. However, there is space to further improve the speed of such adders by retaining the accuracy with minimum error [4]. Thereafter, this inexact speculative adder is fine grain pipelined to reduce the critical path delay that further enhances the operating speed. Subsequently, clock signal fed to various stages of the deep pipelined ISA-architecture has been gated to reduce the power consumption [5]. Speculative adders exploit the fact that the typical carry propagation chain of an addition does not span the whole length of the adder, making it is possible to estimate an intermediate carry using a limited number of previous stages. Thus, the carry propagation chain, which is the critical path of the adder [6], can be split into two or more shorter paths, relaxing constraints over the entire design, reducing glitching power, and improving the Energy-Delay-Area-Product (EDAP) beyond the exact adders.

Design approach of the proposed ISA

With tolerable degradation in accuracy and performance, it is feasible to conceive high-speed, low power and area efficient design using inexact and approximate circuit technique. Accuracy of such circuits can be traded off to improve the speed and power by speculation. Thereby, such adders are referred to as inexact speculative adder [2]. The ISA architecture proposed herein greatly improves hardware efficiency upon the state-of-the-art and introduces a new way to control errors shown in

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figure 1. Taking advantage of such circuits would help to realize extremely energy-efficient and high performance DSPs and hardware accelerators at lower integration cost and with higher speed, data rate or duty-cycling.

This work employs CLA in the suggested architecture, as it has smaller propagation delay compared to the conventional ones. Here, the local sum obtained in parallel from each adder block is not the exact output because the addition has been performed using speculated carry inputs [7]. Correction or Balancing of such sum value is carried out by the compensator block. Adder and compensator blocks are the ones which consume maximum delay along the critical path of the architecture. Thereby, we tend to reduce this delay using the concept of pipelining.

Pipelined carry look-ahead adder

In this design, CLA which is fine grain pipelined to include few logic gates along its critical path and thereby enhancing the frequency of operation. By calculating carry signals advance based upon input bits and does not wait for the input signals to propagate through different stages. Fine grain pipelining can be to increase the processing speed. Also, a CLA is a fast parallel adder as it reduces the propagation delay by more complex hardware, hence it is costlier. Parallel adder is the binary addition of two numbers is initiated when all the bits of the augend and the addend must be available at the same time to perform the computation. To avoid the ripple carry is carry-look ahead which computes some of the carry values directly from the inputs without waiting on the previous carries. If a sequence of bits is all 1's, there will be a carry from the sequence, when it is incremented. Conversely, if there is a 0 anywhere in the sequence, any intermediate carry will be "extinguished" [8]. By feeding the bits into an AND gate, a sequence of all 1's can be detected, and the carry immediately generated.

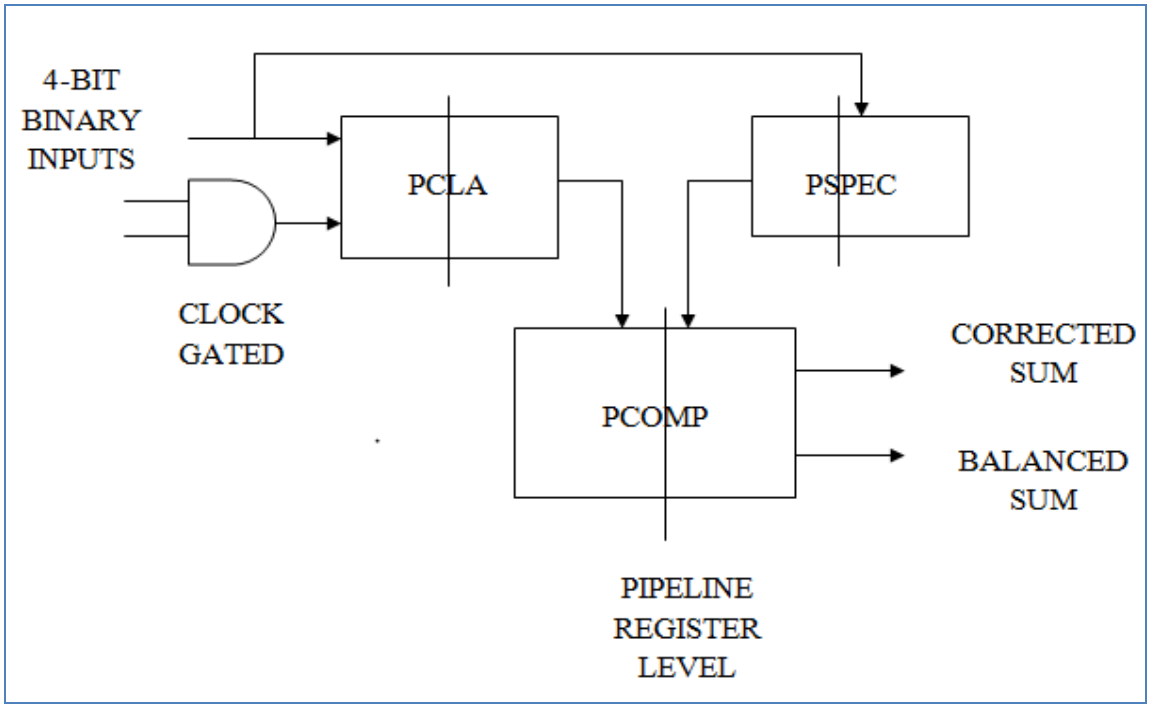

Figure 1. VLSI Architecture for Inexact Speculative Adder

Pipelined speculator

Two n-bit operands for addition are represented as A={A_0,A_1… A_N}, A={B_0,B_1… B_N} whereas, the sum, carry input and carry output are expressed as S=={S_0,S_1… S_N}, Cin and Cout respectively. Gate-level circuit diagram of the speculator used in adder design. This block is based on CLA logic to speculate the output carry for each 4-bit adder block shown in figure 2. Speculation is carried out for 'r' msb bits of each block where r is less than the size of block. Subsequently, the input carry for each speculator block is 0 or 1 which introduces positive or negative errors respectively [9].

The output carry, which is denoted as Cso, from each speculator block is fed as an input carry for the adder block succeeding it. Now, each 4-bit adder block need not wait for the input

carry from the preceding 4- bit adder block. Instead, all such adder blocks perform simultaneous additions on receiving input carries from the concerned speculator blocks. Speculator block computes carry based on the CLA equation.

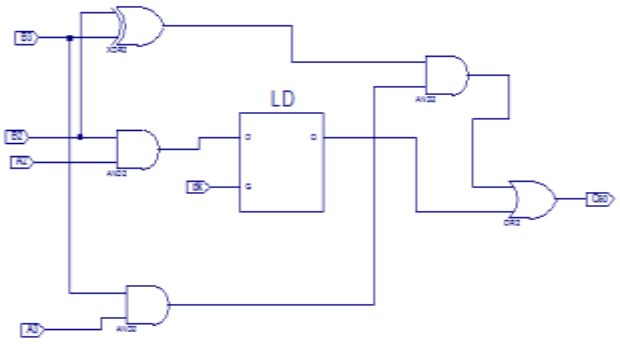

Figure 2. Schematic of Gate Level pipelined speculator

Pipelined compensator

The COMP block detects inconsistencies between speculated carry and expected carry from the previous sub adder with an XOR gate. This creates an error flag that triggers the activation of one of the two compensation techniques, namely error correction and error reduction [10]. The potential error always remains of the same nature as the input carry of the SPEC block. Thereafter, the output from XOR gate generates an error flag (f_e) that triggers the activation of one of the two compensation techniques, error correction and reduction shown in figure 3. If the XOR-gate output is '0' then the local sum is directly passed to the final output. Similarly, if the XOR gate gives '1' then this indicates that an error has occurred which can be either positive or negative.

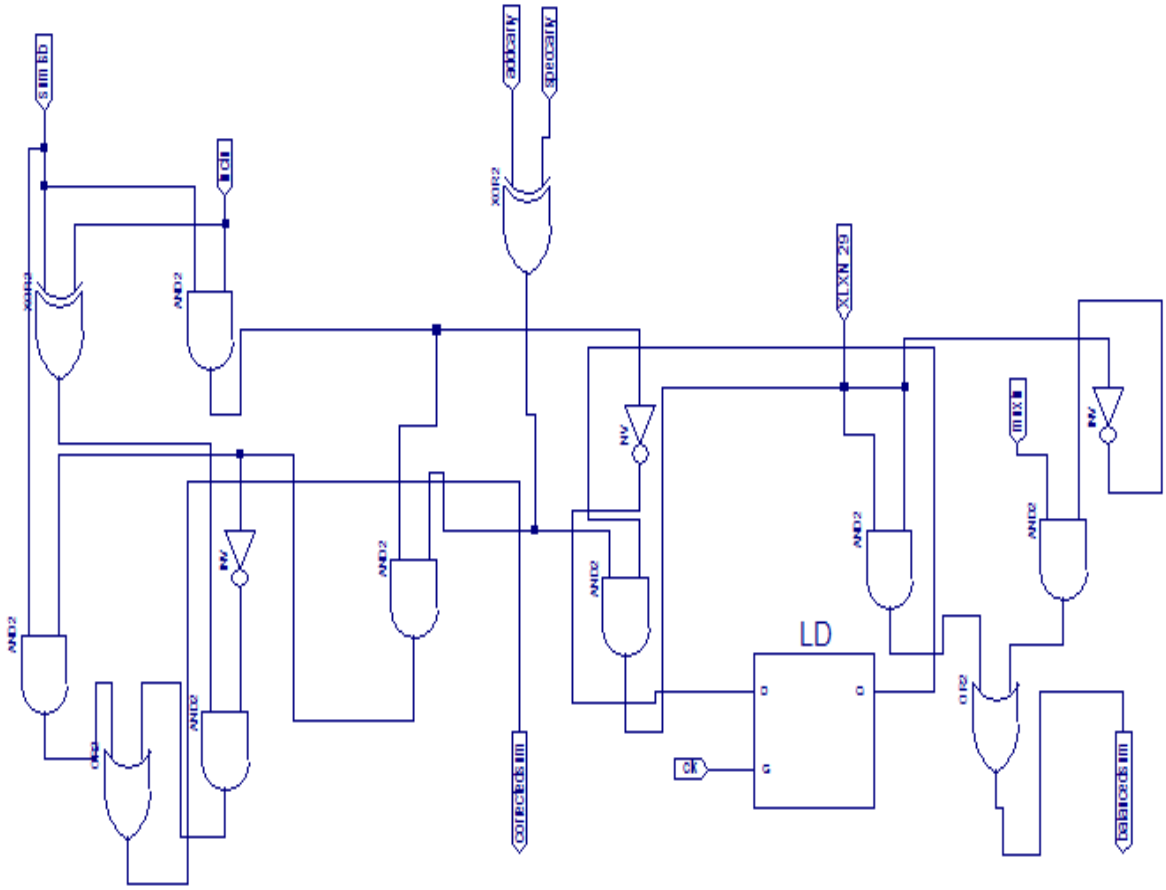

Figure 3. Schematic of Gate level pipelined compensator

Performance analysis of proposed ISA

Schematic representation of proposed PCLA and ISA are shown in figure 4 and 5 respectively. Functional verification is done by Xilinx ISE (Integrated Synthesis Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize their designs, perform timing analysis, examine RTL diagrams, simulate a design reaction to different stimuli, and configure the target device with the programmer. Output of the proposed of ISA is shown in figure 6. Performance analysis of

conventional and proposed ISA in terms of delay and power is given in table 1. Design environment for FPGA products from Xilinx is shown in figure 7 and figure 8, and is tightly coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors.

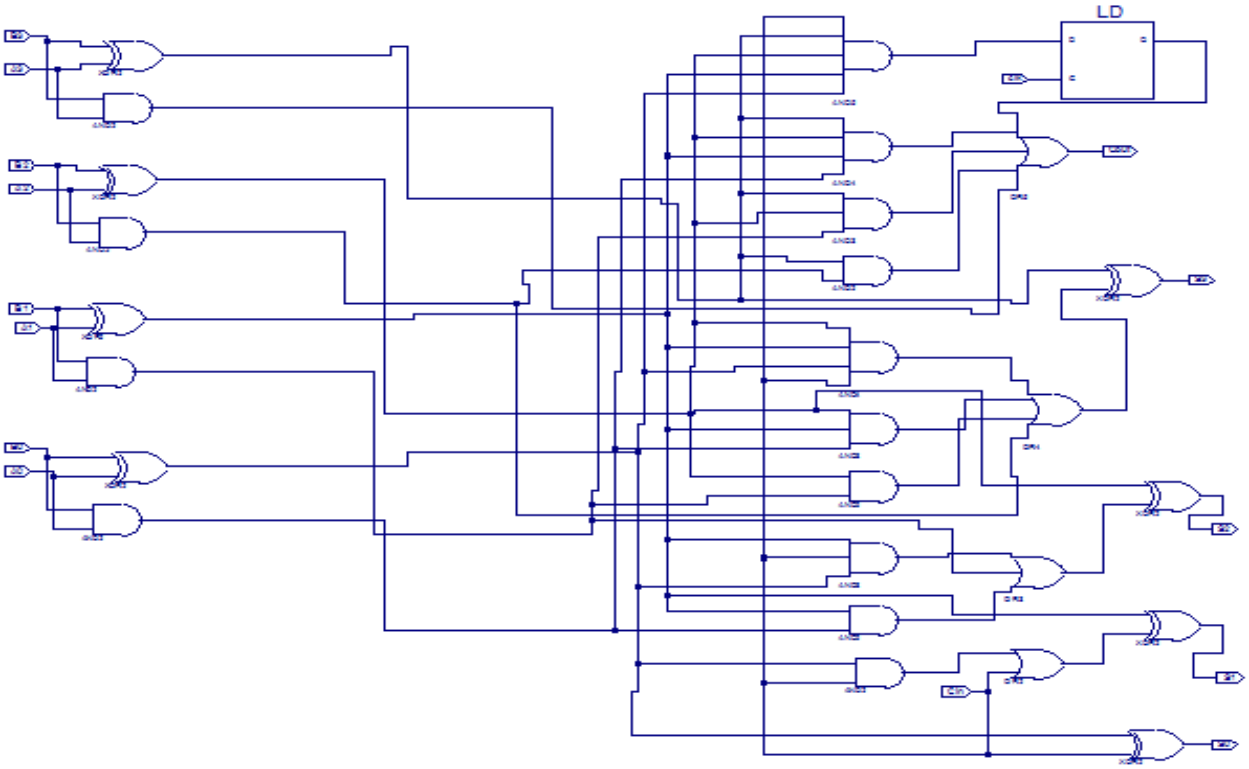

Figure 4. Schematic of proposed PCLA

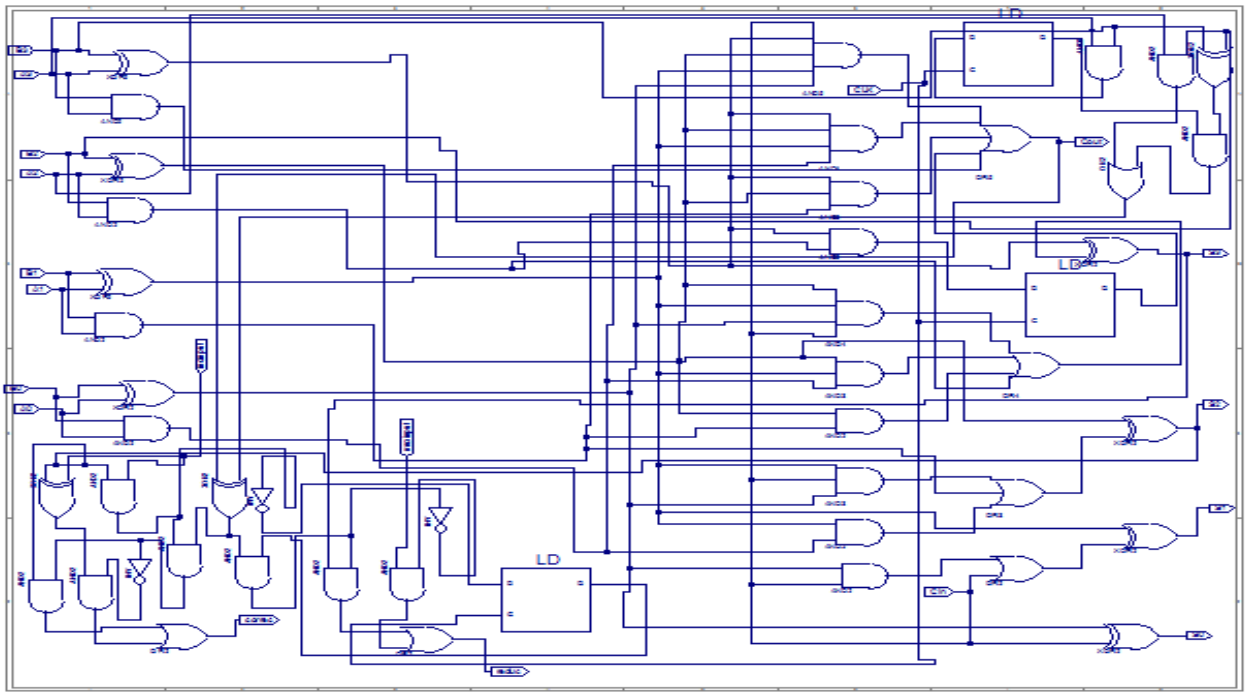

Figure 5. Schematic of proposed ISA

Conclusions

Thus the inexact speculative adder (ISA) has been designed based on carry-look ahead adder (CLA) with high power and low speed. CLA is a fast parallel adder as it reduces the propagation delay and improves the speed. Also, this design is fine grain pipelined and clock gated to escalate speed and alleviate power consumption respectively. Simulation results showed that the proposed ISA can operate lower power and delay compared with earlier. Hardware implementation

of ISA could operate at maximum clock frequency in FPGA.

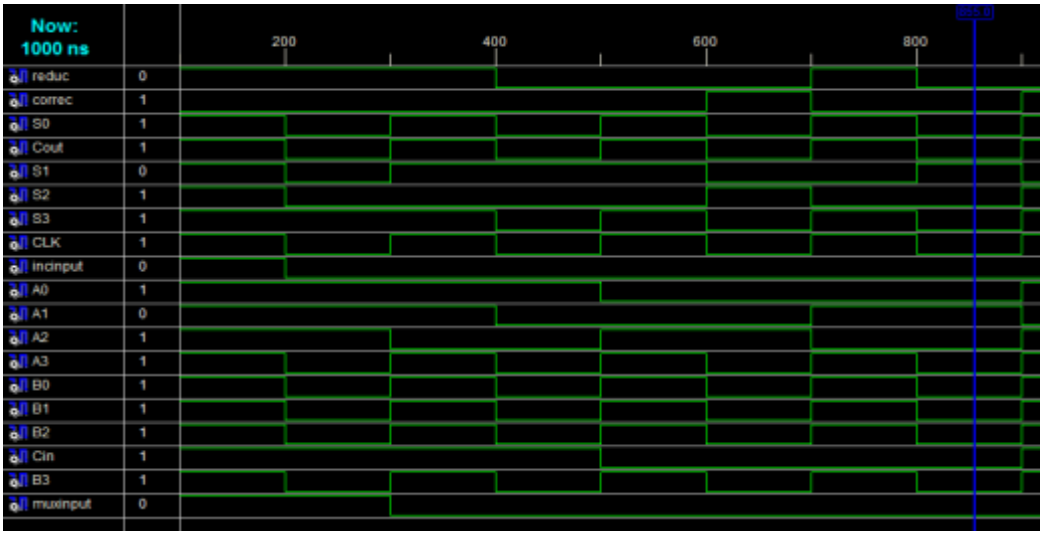

Figure6: Proposed output of ISA

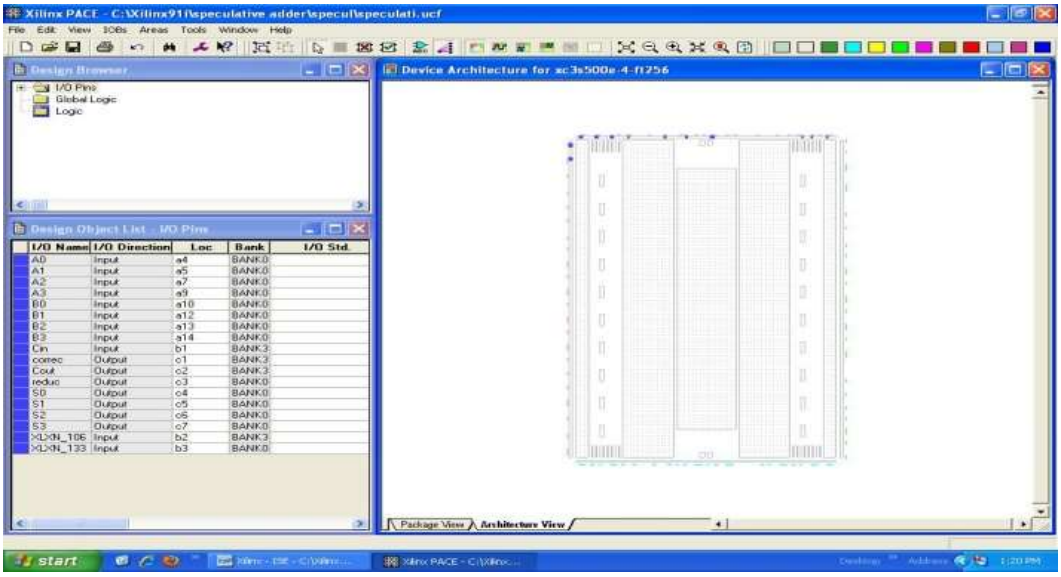

Figure7: Architecture View of ISA

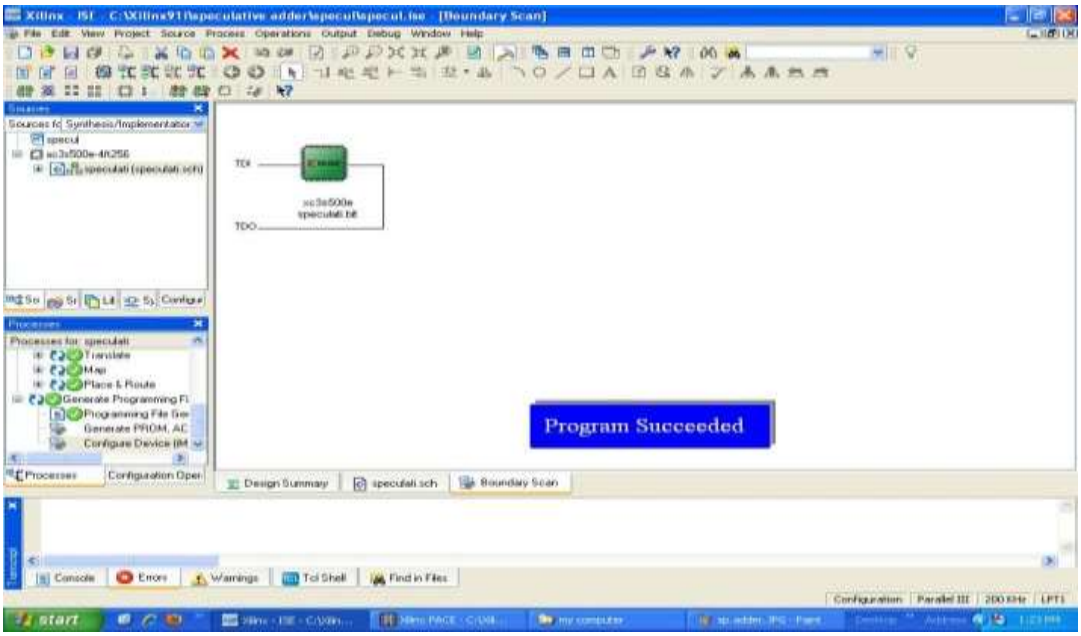

Figure 8. Program verification of ISA

Table 1. Performance Analysis

S. No.	ISA structure	Delay (ns)	Power (mW)
1.	Conventional Inexact Speculative Adder	20.862	81.56
2.	Proposed Inexact Speculative Adder	15.562	60.02

Conflicts of interest

Authors declare no conflict of interest.

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