International Journal of Industrial Engineering, 2018;2(4):89-94.
ISSN: 2456-8449.
http://ijie.gjpublications.com

Research Article

Design of Reversible Arithmetic and Logic unit using Reversible Universal Gate

R. Aarthi*, K. Prasanna

Department of Electronics and Communication Engineering,
Arasu Engineering College, Kumbakonam – 612501. India.

*Corresponding author's e-mail: dhabu12ec001@gmail.com

Abstract

Reversible logic has presented itself as a growing technology which plays an imperative role in quantum computing. Reversible logic has received great attention in the recent years due to their ability to reduce the area which is the main requirement in VLSI Design. The aim of the project is to design area efficient reversible arithmetic and logic unit using reversible universal gate. It minimizes the power and delay. The design of digital circuits in quantum cellular automata poses novel implementation strategies and methodologies are highly desirable. This reversible gates which are applicable in Nano-Technology, Quantum computing, Low power CMOS, Optical computing. QCAD Designer 2.0.3 tool is used for the implementation of quantum cellular automata based reversible circuits. Quantum cellular automata design proves improvement in cell count and area.

Keywords: Quantum Dot cellular Automata; Reversible Circuits; Reversible Universal Gate; Majority Gate; Toffoli Gate.

Introduction

The CMOS technology has some challenging problems in scaling and energy power consumption. So that nano technology is used. But in nano technology energy dissipation is the most significant hurdle. We can make energy dissipation ideally zero, when using Reversible computation [1]. In Reversible computation number of input is equal to number of output. QCA devices perform computation and carry information. Unique feature of QCA is logic values are represented using position of electrons not like voltage level in CMOS. The proposed circuits are constructed using Reversible gates using QCA in QCADesigner [2]. A novel approach to designing efficient QCA-based circuits based on Boolean expressions achieved from reconfiguration of five-input and three-input majority gates [3].

Nanotechnology is the alternative solution to these problems. International Roadmap for Semiconductor (ITRS) accounts several possible alternatives. Quantum dot cellular automata (QCA) can be one of these alternatives. QCA provides a new technique to perform computation and carry information [4]. It is easy to observe and controls the reversible circuits, due to objective properties between inputs and outputs [2]. The proposed decoder is designed using reversible QCA1 gate. QCA1 gate can function as AND-gate as well as OR-gate [5]. The multiplexer is a combinational circuit which permits picking one output amid numerous inputs. It transfers one of the inputs to the output at a time, so it is also known as Data selector. This type of operation facilitates to share one costly device for more than one application in a system. Due to its abundant use, it has become necessary to implement a multiplexer circuit which is area efficient which results in the reduction of the cost of designing [6].

Landauer demonstrated in the early 1960s, irreversible hardware computation results in energy dissipation due to the information loss, regardless of its realization technique. Landauer has shown that for irreversible logic computations, each bit of information lost generates kTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which the computation is performed [7]. The basic elements in QCA are cells; each cell is composed of two mobile electrons that are located in opposite corners according to columbic energy, resulting in two

Received: 02.04.2018; Received after Revision: 15.04.2018; Accepted: 16.04.2018; Published: 29.04.2018

possible polarizations (P = +1, P = −1) [7]. A cost effective realization of 2: I multiplexer is introduced to outperform the efficiency of existing designs [8]. The most impressive function of reversible logic lies in quantum computing and it can be implemented through quantum dot cellular automata [9]. Normally we simulate verilog coding in XILINX ISE and simulated the waveforms. Area requirements analysed using Quartus II software. It takes area size in um^2. The coding may be in gate level, Behavioral level, or structural level.

Proposed work

Mostly the system architecture uses AND,OR and NOT gate for circuit design. It can be driven from 3 input majority gate. The 3 input majority gate has 3 inputs and 1 output and polarization states. It is shown in fig. 1. The AND, OR and NOT driven from 3 input majority gates. It can be easily constructed. The 3 input majority gate is shown in fig. 1.

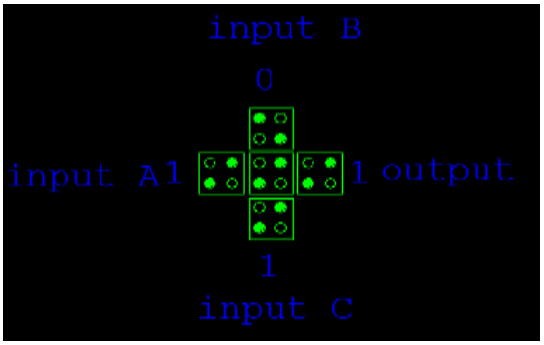

Fig. 1. 3-input Majority Gate

Logic function of majority gate is

Y=AB+BC+AC

Y= MV(MV(sel',a,0),MV(sel,b,0),1)

= a.sel'+b.sel

Proposed design of 2:1 reversible multiplexer

The proposed 2:1 multiplexer has two inputs a and b, one select line sel and single output y. If select line sel=O, input a is selected, and when sel=1, input b performs at the output. The majority voter illustration of the function is as followed. The truth table for 2:1 Multiplexer is given in table 1. It is constructed using 2 AND and OR gates using QCA wire connection as shown in fig. 2.

Table 1. Truth table for 2:1 multiplexer

Sel0	Sel1	output
0	0	D
0	1	C
1	0	B
1	1	A

Proposed design of reversible universal gate

The proposed design of Reversible Universal gate uses Majority voter gate and 2:1 Multiplexer logics. It takes 3 inputs and 3 outputs. The inputs are (A, B, C) and outputs are (P, Q, R). The number of inputs and outputs are same as shown in fig. 3.

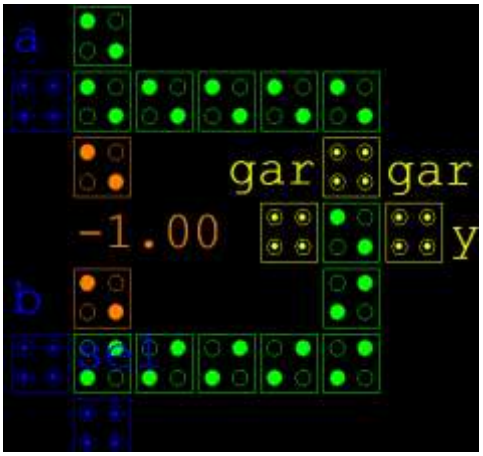

Fig. 2. Proposed 2:1 multiplexer QCA design

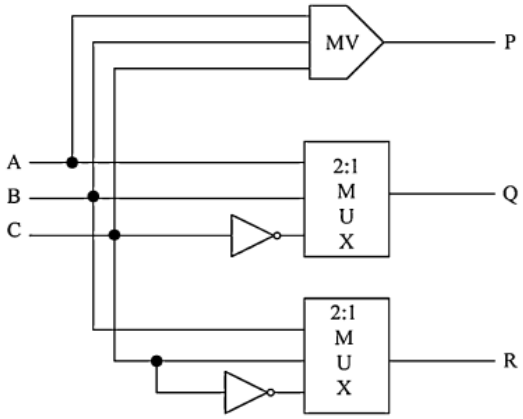

Fig. 3. Proposed 1:2 reversible universal gate schematic diagram

Inverters are depicted in schematic diagram. Fan Outs are allowed in QCA implementation. The Reversible Universal Gate consists of 211 Quantum Dot cells covering an Area of 0.23 nm^2. Bistable Approximation simulation type is used, for simulating Reversible Universal Gate. 2:1 Reversible Multiplexer is used as the basic block diagram of Universal Gate. QCA implementation of Reversible Universal Gate is shown in fig. 4.

Proposed design of reversible arithmetic unit

The proposed design of Reversible Arithmetic Unit uses one Toffoli gate and two RUG to deliver functions like increment, Decrement and Constant (0, 1). The design has 5 inputs and 5 outputs, which comprises garbage outputs (G1, G2, G3) and select lines (C0, C1,

C3) shown in table 2. Schematic diagram of Arithmetic circuit is shown in fig. 5.

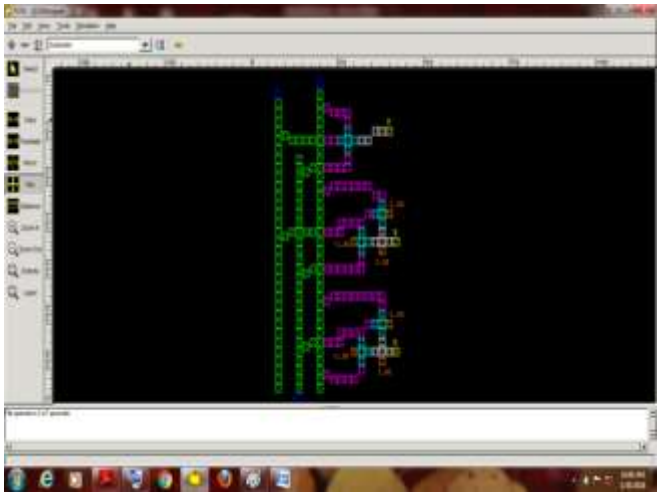

Fig. 4. Proposed QCA design of reversible universal gate

Table 2. Truth table for reversible arithmetic unit

C0	C1	C2	F
0	0	0	B
0	0	1	A+B
0	1	0	B+1
0	1	1	A+B+1
1	0	0	B
1	0	1	A+B
1	1	0	B-1
1	1	1	A+B+1

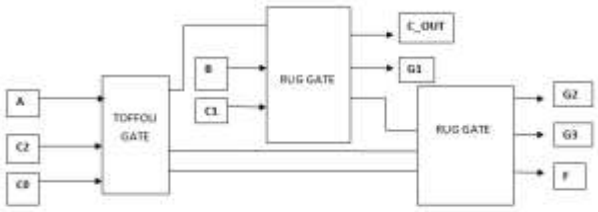

Fig. 5. Proposed reversible arithmetic unit schematic diagram

The proposed design of Reversible Arithmetic Unit consists of 841 Quantum dot cells and covers Area 1531623.79 nm^2. QCA Design of Arithmetic circuit is shown in fig 6. The truth table shows functions like,

Increment - A+B+1
Decrement - A+B-1
Addition - A+B

Proposed design of reversible logic unit

The proposed design of Reversible Logic Unit consist of 1027 Quantum dot cells and covers Area 2661338.34 nm^2. QCA Design of Logical unit is shown in fig. 7. Schematic diagram of logic circuit is shown in fig. 8. The truth table 3 shows functions like

NOT - A'+B+1
AND - (A.B)
OR - (A+B)
NOR - (A+B)'
XOR - A XOR B
COPY - A (or) B

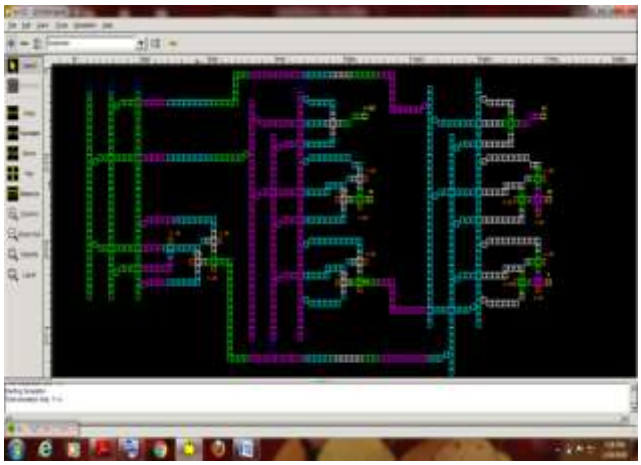

Fig. 6. Proposed QCA design of reversible arithmetic unit

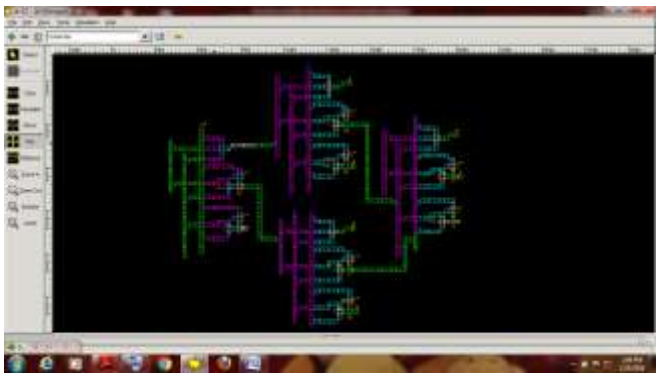

Fig. 7. Proposed QCA design of reversible logic unit

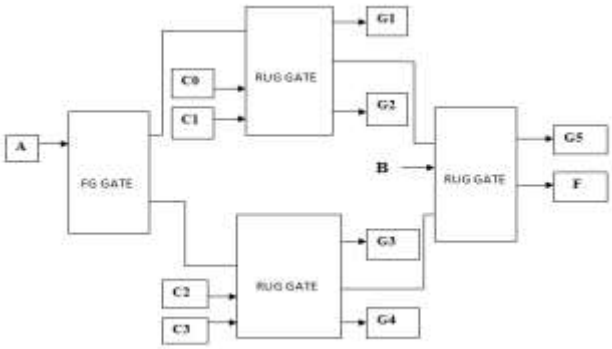

Fig. 8. Proposed reversible logic unit schematic diagram

Proposed design of reversible arithmetic and logic unit

Arithmetic Logic Unit used as a building block for many devices. Main aim is to

maximize logical operations and minimize the select lines. The Reversible ALU subdivided into 2 submodules (i.e.) Reversible Arithmetic Unit and Reversible Logic Unit. A select line is used to select output from either of the two modules connected to a rug at the output end. The ALU is constructed using Arithmetic Unit and Logic Unit modules. Arithmetic Unit output denoted as F1 and Logic Unit output denoted as F2. Schematic and its QCA design are shown in fig. 9 and 10. The arithmetic unit shows that incrementation, decrementation and copy in its output result. It verified by truth table 4.

Table 3. Truth table for reversible logic unit

SEL	F1	F2	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

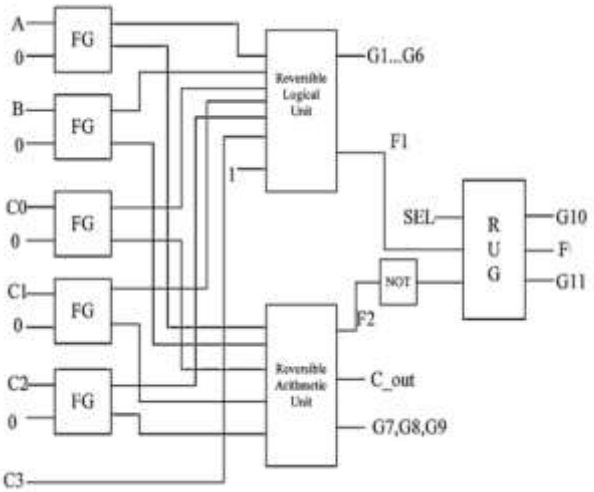

Fig. 9. Proposed reversible arithmetic and logic unit schematic diagram

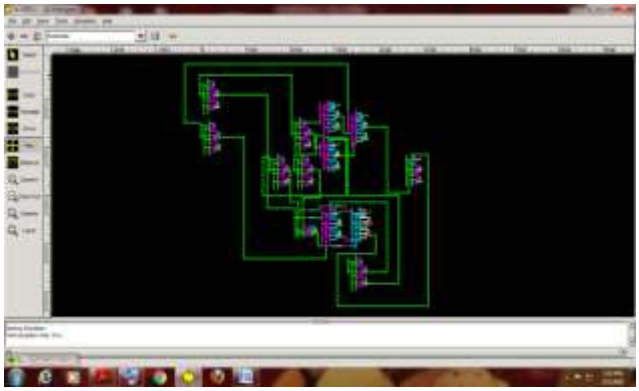

Fig. 10. Proposed QCA design of reversible arithmetic and logic unit

Table 4. Truth table for reversible arithmetic and logic unit

C0	C1	C2	C3	F	Function	
0	0	0	0	0	A’	NOT
0	0	1	0	0	(A.B)	AND
0	1	0	0	0	(A+B)’	NOR
0	1	0	1	1	CONSTANT	
0	1	1	0	1	B’	NOT
1	0	0	1	0	B	COPY
1	0	1	0	1	CONSTANT	
1	0	1	1	1	(A+B)	OR
1	1	0	0	1	(A XOR B)	XOR
1	1	0	1	1	(A.B)’	NAND
1	1	1	1	1	A	COPY

Results and discussion

The arithmetic unit shows that incrementation, decrementation and copy in its output result.

E.g. when input A=0, B=0
Selection input C0=0, C1=1, C
Output F=A+B+1 (incrementation)
F=1 in (fig. 11).

It performs basic logic functions like AND, NOT, NOR, XOR and Constant output.

E.g. when input A=1 B=0
Sel input C0=0, C1=1, C2=0 and C3=0
Output F=A.B (AND)
F=0 in (fig. 12)

Arithmetic Unit and Logic Unit output is given to Universal Gate with Selection input for desired Output.

E.g. input F1=1 F2=1
Selection input Sel=1
Output F=1 in (fig. 13)

Reversible Arithmetic unit uses Toffoli gate for input selection and its output obtained from Reversible universal gate. It is denoted by F. QCA design contains 841 Quantum dot for generating Arithmetic circuit. Reversible logic unit uses Feynman gate for input selection and its output obtained from Reversible Universal Gate. Its output denoted by F. QCA design contains 1027 Quantum dots for generating Logic circuit. Reversible Arithmetic and logic unit constructed by 2 modules, namely Arithmetic and Logic circuits. It uses 5428 quantum dots for generating Reversible ALU circuit. Table 5 shows the proposed design that consumes nanometer square area. But in existing system, which is simulated using Xilinx software that uses micrometer square area.

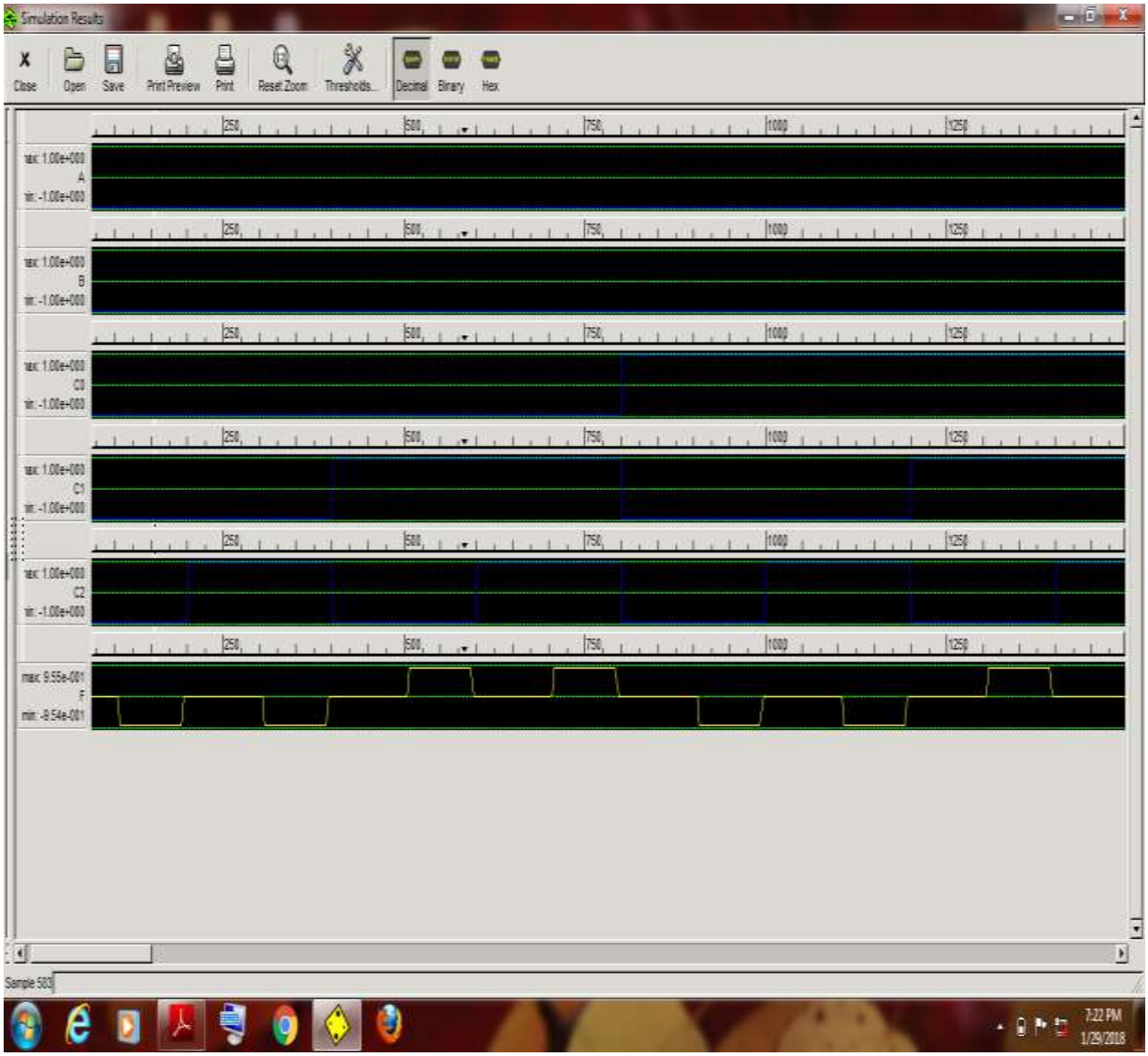

Fig. 11. Result of reversible arithmetic unit

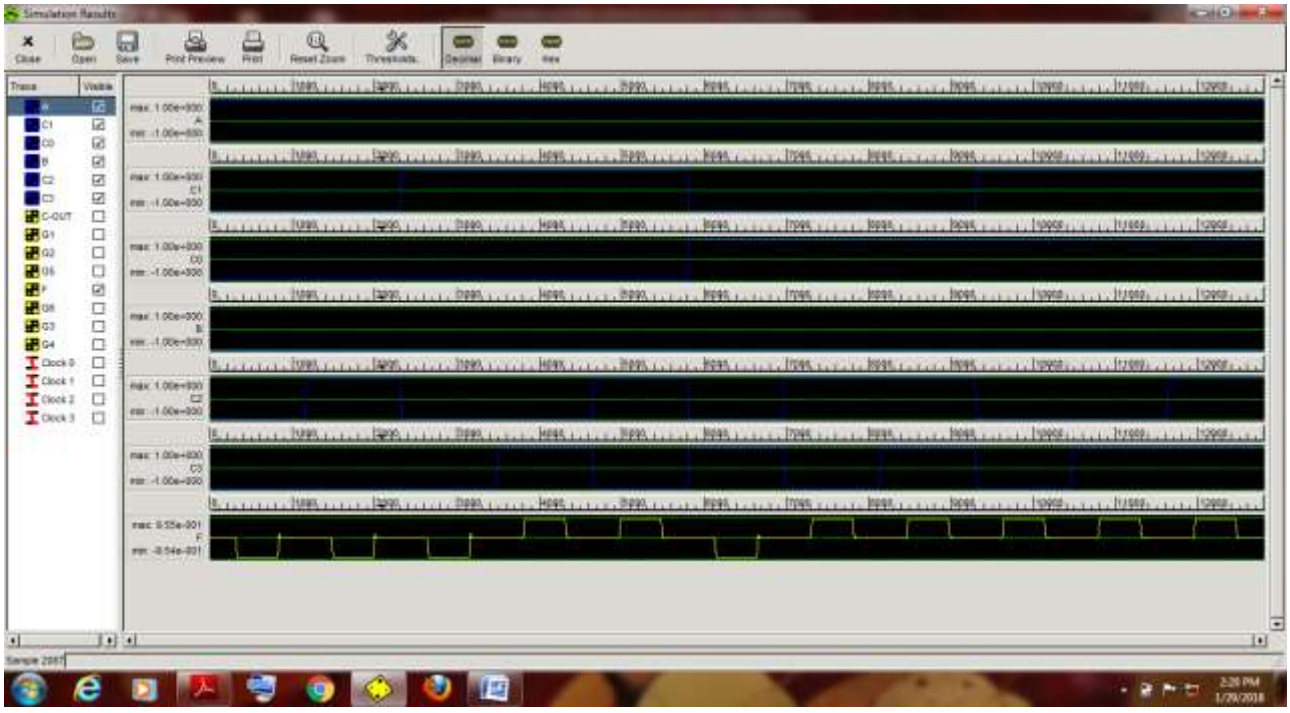

Fig. 12. Result of reversible logic unit

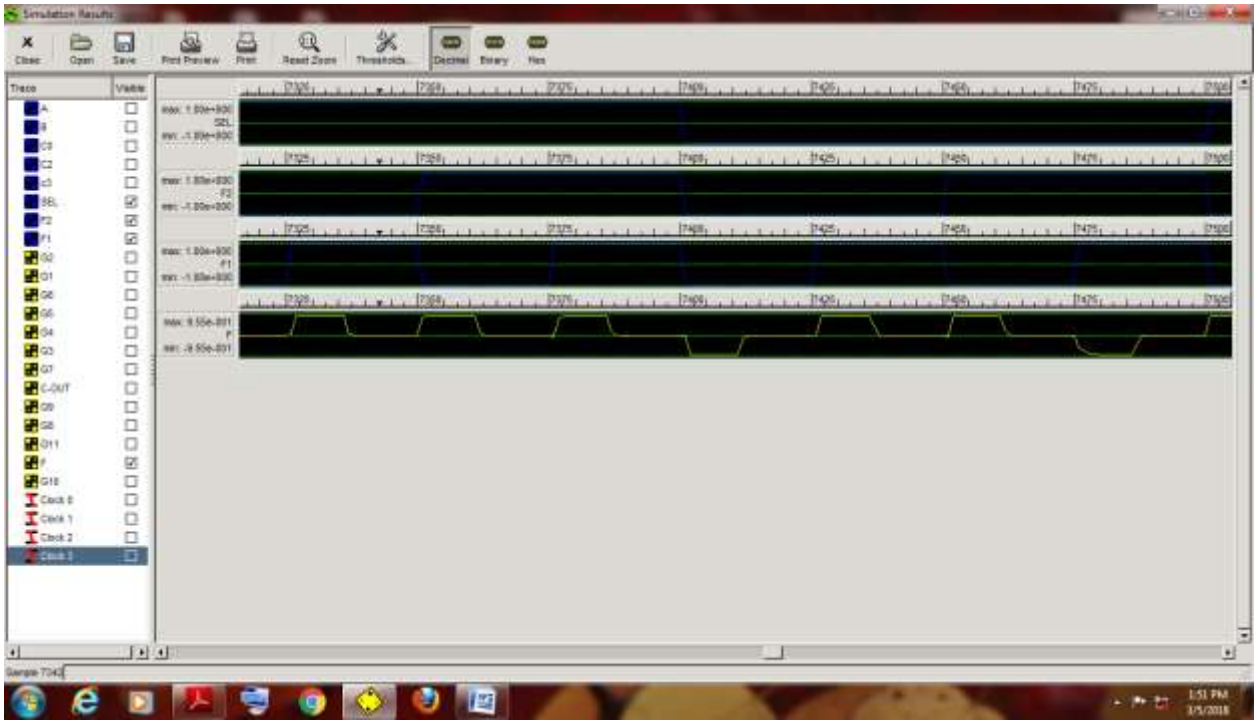

Fig. 13. Result of reversible arithmetic and logic unit

Table 5. Area estimation of Reversible Circuits

Circuit design		Area (um^2)
ALU	Conventional Circuit	4.8
	Proposed Reversible Circuit	2728788

Conclusions

The present work demonstrated QCA based novel nano scale reversible circuits. The new layout of QCA is denser than existing circuits. It shows that QCA is alternative platform to CMOS, for implementing Reversible circuits. Truth table based comparison of simulation results established the design accuracy. The proposed circuits can be used to design reversible architecture for nano communication systems.

Conflicts of Interest

Authors declare no conflict of interest.

References

[1] Ritjit M, Sandeep S. A novel design of reversible 2:4 decoder. International Conference on Signal Processing and Communication; 2015, Noida, India.

[2] Hashemi S, Keivan N. Reversible Multiplexer design in Quantum dot cellular automata. Journal of Advanced Research. 2014;3:523-28.

[3] Chabi AM, Say Edsalehi S, Angizi S, Navi K. Efficient QCA Exclusive-or and Multiplexer circuits based on a nanoelectronic compatible designing approach. International scholarly research notices; 2014;2014:Article ID 463967.

[4] De D, Bhattacharya S, Ghatak KP. Quantum dots and Quantum dot cellular automata: Recent Trends and Application. Physics Research and Technology. NY 11788; USA: Nova Science Publishers. Inc. 2013.

[5] Das JC, De D, Sadu T. A Novel low power nano scale Reversible decoder using Quantum dot cellular Automata for nano communication. International Conference on Devices, Circuits and Systems; 2016, Coimbatore, India.

[6] Kianpour M, Nadooshan RS. A Novel decoder implementation in Quantum dot cellular automata. International Conference on Nanoscience, Technology and Societal Implications; 2011, Bhubaneswar, India.

[7] Landauer R. Irreversability and heat generation in the computational process. IBM Journal of Research. 1961;5(3):183-91

[8] Shafi MA. Islam S. Bahar A N. A Review of Reversible logic gate and its QCA implementation. International Journal of Computer Applications. 2015;128(2):27-34.

****

